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The frequency and voltage dependent electrical characteristics of Al–TiW–Pd_2Si/n-Si structure using I–V, C–V and G/ω–V measurements

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Abstract

The forward and reverse bias capacitance–voltage (C–V) and conductance–voltage (G/w–V) characteristics of Al–TiW–Pd_2Si/n-Si structures have been investigated over a wide frequency range of 5 kHz–5 MHz. These measurements allow to us the determination of the interface states density (N_{ss}) and series resistance (R_s) distribution profile. The effect of R_s on C and G is found noticeable at high frequencies. The C–V–f and G/w–V–f characteristics of studied structures show fairly large frequency dispersion especially at low frequencies due to N_{ss} in equilibrium with the semiconductor. The N_{ss} profile was obtained both forward bias current–voltage (I–V) characteristics by using into account the bias dependent of the ideality factor and effective barrier height (Φ_e) and low frequency (C_{LF})–high frequency (C_{HF}) method. The plot of series resistance vs. voltage for the low frequencies gives a peak, decreasing with increasing frequencies. The frequency dependent C–V and G/w–V characteristics confirm that the R_s and N_{ss} of the Al–TiW–Pd_2Si/n-Si structures are important parameters that strongly influence the electric parameters in device.

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Keywords: MS structure; Frequency dependent; Interface states; Series resistance; Pd_2Si/n-Si contacts

1. Introduction

The formation process of silicide compounds between metal and semiconductor is of interest because of the potential electronic devices applications and the need for basic understanding of the properties of metal–semiconductor (MS) interfaces. Knowledge of the electrical characteristics of the silicide at the interfaces is important for understanding the formation of Schottky barriers and interface states between silicide and Si interfaces. Aluminum and platinum silicide have most widely used small area metallic contacts on Si substrate [1–4]. Palladium silicide (Pd_2Si) offers a useful alternative to Al–PtSi as a contact material. Pd_2Si/Si contacts are similar in electrical behavior to PtSi/Si contacts, but can be fabricated at much lower temperatures. PtSi contacts suffer from a number of processing difficulties associated with the Pt because of its high melting temperature. The idea of using palladium silicide contacts on Si substrate is not new. However there is a little experimental information in the literature about them.

The interface properties, frequency and voltage dependent some electrical parameters such as interface states and series resistances obtained from current–voltage (I–V) and admittance–voltage (C–V and G/w–V) characteristics of metal–semiconductor structures (MSs) have been subject of both experimental and theoretical studies in the past decades [4–20]. Usually, the forward bias current–voltage (I–V) characteristics are linear in the semi-logarithmic scale at low voltages but deviate considerably from linearity due to the effect of device parameters, such as the R_s and N_{ss} when the applied voltage is sufficiently

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large [21,22]. Due to the technological importance of MSs, a full understanding of the nature of their electrical characteristics is of great interest. A complete description of R_s and N_{ss} effect on I–V, C–V and G/w–V characteristics of MS and metal–insulator–semiconductor (MIS) type structures is still a challenging problem [23–26]. The values of I, C and G depend on various parameters, such as density of interface states, series resistance, insulator layer thickness and barrier height formation and preparation of devices. Among them, N_{ss}, R_s and insulator layer at M/S interface significantly can alter the device I–V, C–V and G/w–V characteristics from their ideal behavior and make the measured C and G strongly frequency dependent especially at low and intermediate frequencies in the depletion and accumulation region. The interface states can easily follow the ac signal, at low frequencies and yield an excess capacitance, which depends on the relaxation time of the interface states and the frequency of ac signal. In contrary, at high frequencies the charges at the surface states cannot follow an ac signal. These interface states usually lead to a bias shift and frequency dispersion of the capacitance–voltage (C–V) and conductance–voltage (G/w–V) curves [23]. Therefore, it is important to include the effect of the frequency and examine detail the frequency dispersion of capacitance and conductance characteristic. Also the analysis of the C–V and G/w–V characteristics of these devices obtained only at one frequency does not give detailed information about the electrical characteristics.

MS and MIS structures formed by depositing various metals on the Si have been studied over a wide frequency and temperature ranges [7,14]. However, only a few reports exist on palladium silicide based diodes [24–26]. Chin et al. [24] studied Pd_2Si SBDs on n-type Si at 300 K and p-type Si at 80 K only. Chand and Kumar [26] investigated various aspects of Pd_2Si/p-Si Schottky diodes in the temperature range of 60–200 K.

The aim of this study is to investigate experimentally the frequency dependence of the forward and reverse bias C–V and G/w–V characteristics of Al–TiW–Pd_2Si/n-Si structures by considering the R_s and N_{ss} effect. Therefore, in this study the frequency dependent of the forward and reverse bias C–V and G/w–V measurements of Pd_2Si/n-Si (1 1 1) (MS) structures have been carried out in over a wide frequency and bias voltage range from 5 kHz to 5000 kHz and from −4 V to 10 V, respectively. To determine accurate values of R_s and N_{ss} of the Al–TiW–Pd_2Si/n-Si structures, we have applied the method by Nicollian and Brews [7]. Also, the N_{ss} distribution profile of MS structure as a function of E_c–E_{ss} was obtained from the forward bias I–V data. Experimental results show that both N_{ss} and R_s are important parameters that influence the electrical characteristics of MS structures.

2. Experimental procedure

The Al–TiW–Pd_2Si/n-Si structures were fabricated on 2 in. diameter n-type (P doped) single crystal silicon wafer with (1 1 1) surface orientation, 0.7-Ω cm resistivity and 3.5 μm thickness. The pattern of these structures were fabricated by lift-off of litho-graphically system, defined as photo-resist, and annealed at 500 °C for 1 min in flowing dry nitrogen (N_2) ambient in a rapid thermal annealing furnace. Thus produced chip contains 14 Al–TiW–Pd_2Si/n-Si structures with the areas of changing 1×10^{-6} cm^2 to 14×10^{-6} cm^2. Only the results of diode with the area of 8×10^{-6} cm^2 are presented in this paper.

For the fabrication process the Si wafer first was cleaned in a mix of a peroxide-ammoniac solution in 10 min and subsequent quenched in de-ionized water of resistivity of 18 MΩ cm for a prolonged time. After the cleaning process, high purity (99.999%) Al with a thickness of about 2000 Å were thermally evaporated onto whole back side of Si wafer at a pressure about 10^{-6} Torr in high vacuum system. The ohmic contacts were formed by annealing them for a few minutes at 450 °C. To fabricate Pd_2Si–nSi layer, palladium was deposited on Si wafer by using thermal evaporation method until the thickness of Pd_2Si film was about 0.6 μm, subsequently annealed at 573 K for 15 min.

To form the metal electrodes (rectifier and ohmic contacts), traditionally Al dot could have been formed on Pd_2Si–nSi structure. But Al has high diffusion ability and it can lead to degrade contact's quality. Therefore in this work, to prevent the disadvantage of Al diffusion to n-Si, the TiW alloy played the role of the diffusion barrier between Pd_2Si, and Al was deposited on Pd_2Si–nSi layer. For this process, the sandwiched structure Al–$Ti_{10}W_{90}$ was deposited by the magnetron sputtering method at temperature of 420 °C in vacuum system 'Oratoria-5' and then annealed at temperature of 500 °C in nitrogen atmosphere (N_2) for 20 min. Prior to the deposition, vacuum and target conditions were performed. Taking into account the dispersion factor of Ti and W, the compound target (Ti 10%, W 90%) were made. The deposition chamber was pumped down to the ultimate vacuum and repeatedly charged with argon and pumped down in order to minimize the residual gas components. The alloy compound target film was bombarded by Ar^+ ions with high energy at room temperature until the thickness of $Ti_{10}W_{90}$ film on Pd_2Si–nSi substrate was about 0.2 μm. The base pressure during the ion bombardments was about 10^{-6} Torr. Al was also deposited onto TiW–Pd_2Si/n-Si structure by the same method until the thickness of Al film on $Ti_{10}W_{90}$–Pd_2Si–nSi layer was about 1 μm.

The current–voltage (I–V) measurements were performed by the use of a Keithley 220 programmable constant current source and a Keithley 614 electrometer at room temperature. The C–V and G/ω–V measurements were performed in the frequency range of 5 kHz–5 MHz by using a HP 4192A LF impedance analyzer and small sinusoidal test signal of 20 mV_{p-p} from the external pulse generator is applied to the sample in order to meet the requirement [7]. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

When a MS contact with series resistance R_s is considered, the current through a barrier can be given by the following relationship [21,22]

$$I = I_0 \exp\left(\frac{q(V - IR_s)}{nkT}\right)\left[1 - \exp\left(\frac{-q(V - IR_s)}{kT}\right)\right] \quad (1a)$$

where I_0 is the reverse saturation current and is equal to

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{B_0}}{kT}\right) \quad (1b)$$

where A is the rectifier contact area, A^* is the effective Richardson constant and it is taken as 120 A/cm^2 K^2 for n-type Si [22], k is the Boltzmann constant, Φ_{B_0} is the zero-bias barrier height and T is the temperature in K. Fig. 1. shows the semi-logarithmic I–V characteristics of the Al–TiW–Pd_2Si/n-Si structure, measured at room temperature. The values of I_0 were obtained by extrapolating the linear region of the ln I–V curve to zero applied voltage and the Φ_{B_0} value was calculated Eq. (1b). The values of ideality factor n and zero bias barrier height Φ_{B_0} obtained are 2.8 and 0.653 eV, respectively, at room temperature. The value of Φ_{B_0} is in good agreement with value of obtained by Kircher [1] and Studer [3] for Pd_2Si/Si diodes.

When preparing the sample to prevent the disadvantage of Al diffusion to nSi, the TiW alloy was deposited on Pd_2Si–nSi layer. But as shown in Fig. 1 the value of forward current ratio to reverse current is about 6 at ±1.5 V. That is to say the rectifying ratio is lower than expected value and the value of ideality factor is greater than unity. These results can be originated from the interfacial insulator layer formation at interface and particular

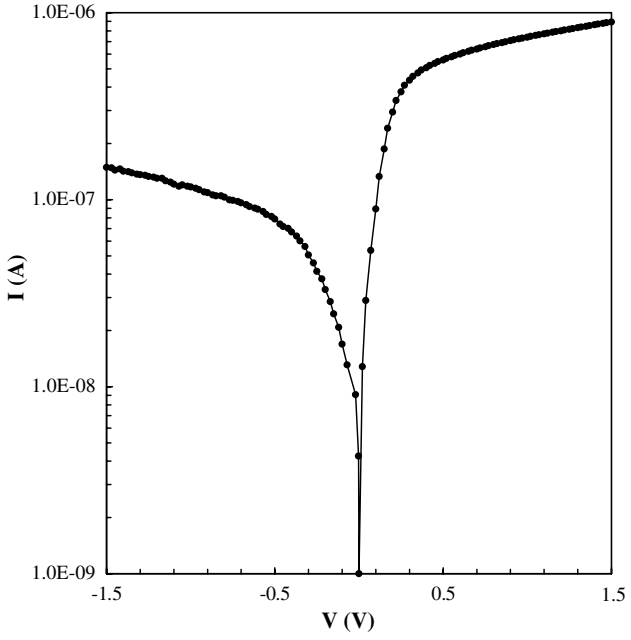

Fig. 1. The forward and reverse bias I–V characteristics of the of Al–TiW–Pd_2Si/n-Si structure at room temperature.

distribution of interface states. The voltage dependent of ideality factor and effective barrier height (Φ_e) are calculated from the forward bias ln (I)–V plot and can be written following equations, respectively [15]

$$n(V) = \frac{q}{kT}\left[\frac{(V - IR_s)}{\ln(I/I_0)}\right] = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \quad (2)$$

$$\Phi_e = \Phi_{B_0} + \beta(V - IR_s) = \Phi_{B_0} + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \quad (3)$$

where β is the voltage coefficient of the effective barrier height Φ_e. The expression of Eq. (2) is identical to Eq. (18) of Card and Rhoderick [5] and the expression for the interface state density is reduced to

$$N_{ss}(V) = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{W_D}\right] \quad (4)$$

where δ is the thickness of interfacial insulator layer, W_D is the width of the space charge region, ε_i and ε_s are the permittivity of the interfacial insulator layer and the semiconductor, respectively. Furthermore in n-type semiconductors, the energy of interface states N_{ss} with respect to the bottom of conduction band E_c at the surface of the semiconductor can be obtained according to Refs. [21,22].

The natural interfacial layer thickness δ was obtained from high frequency (1 MHz) C–V characteristics using the equation for insulator layer capacitance ($C_{ox} = \varepsilon_i\varepsilon_0 A/\delta$), where $\varepsilon_i = 3.8\varepsilon_0$ [6,22]. The W_D was also calculated C–V characteristic at 1 MHz using the equation for the width of the space charge region ($W_D = [2\varepsilon_s\varepsilon_0 V_d/qN_D]^{1/2}$), where $\varepsilon_s = 11.8\varepsilon_0$ [7,21,22] and V_d is the diffusion potential. Furthermore, in n-type semiconductors, the energy of the interface states E_{ss} with respect to the bottom of the conduction band at the surface of semiconductor is given by

$$E_c - E_{ss} = q(\Phi_e - V) \quad (5)$$

Substituting in Eq.(4) the values of the voltage dependence of n (V), $\delta = 3.81$ Å, $\varepsilon_i = 3.8\varepsilon_0$, $W_D = 0.385$ μm, $\varepsilon_s = 11.8.4\varepsilon_0$ [7,22], the N_{ss} profile was obtained as a function of (E_c E_{ss}) and are given in Fig. 2. As shown in Fig. 2, the exponential growth of the N_{ss} from midgap towards the bottom of conduction band is very apparent. The density distribution curve of the interface states is in the range (E_c − 0.54) to (E_c − 0.64) eV.

Fig. 3 shows the experimental measurement capacitance (C_m) and conductance (G_m/w) of Al–TiW–Pd_2Si/n-Si structure in the frequency range from 5 kHz to 5 MHz with a small ac signal of 20 mV$_{rms}$ peak to peak amplitude at room temperature. The values of C_m and G/w vary from the strong inversion region (−4 V) to the strong accumulation region (10 V). Fig 3a and b show that the rapid decreasing of both C_m and G_m/w with frequency, respectively at the positive biases. These changes occur especially at the low-frequencies and depletion region while the high-frequency capacitance and conductance remain almost constant. In other words, in the high frequency, the N_{ss}

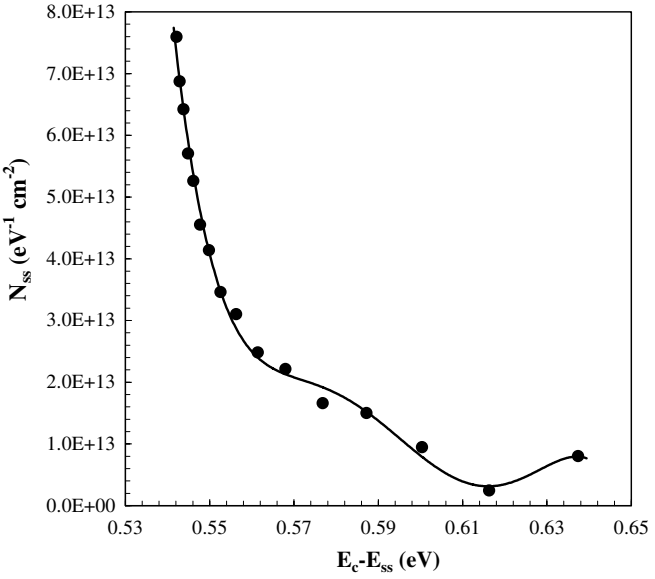

Fig. 2. The energy distribution profile of the N_{ss} with obtained from the forward bias I–V characteristics of the Al–TiW–Pd_2Si/n-Si structure at room temperature.

cannot follow the ac signal and consequently do not contribute appreciably to the Al–TiW–Pd_2Si/n-Si structure capacitance.

As a result, we can say that in the low frequencies N_{ss} can follow the ac signal and yield an excess capacitance and conductance, which depends on the frequency. But at the efficiently high frequencies ($f > 100$ kHz), the interface states cannot follow the ac signal. In addition the values of conductance give peaks at low frequencies and this anomalous peak has a tendency to disappear at high frequencies. Such behavior indicates that there are various kinds of interface states with different life times and they can follow an ac signal at low frequency, but cannot follow at high frequencies.

In recent years, several methods have been suggested to determine the series resistance of MS, MIS and MOS structures [7,27,28]. According to a method presented by Nicollian and Brews [7], the real series resistance of the MS and MIS structures can be calculated from the C_m and G_m in strong accumulation region at high frequencies ($f \geqslant 1$ MHz) [2] as

$$R_s = G_{ma}\left(G_{ma}^2 + (\omega C_{ma})^2\right)^{-1} \quad (6)$$

In this study, the frequency and voltage dependent series resistance profile of Al–TiW–Pd_2Si/n-Si structures subtracted from the measurement capacitance C_m–V and G_m/w–V data at each frequency by using admittance technique [7]. In addition, the voltage and frequency dependence of the R_s can be obtained from the measurements of C_m–V–f and G_m/w–V–f curves for any voltage. The values of R_s were calculated according to Eq. (6) and are shown in Fig. 4 for various frequencies. These very significant values demanded that special attention be given to effects of the series resistance in the application of the

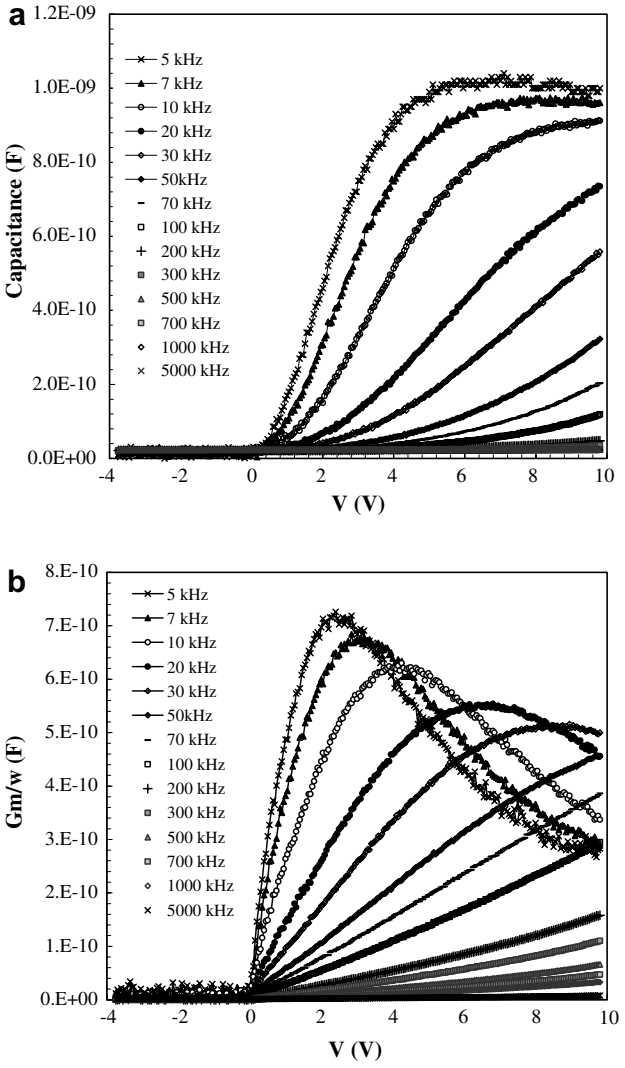

Fig. 3. (a) The measured capacitance C (V,f) and (b) conductance G/w (V, f) for Al–TiW–Pd_2Si/n-Si structure at room temperature.

admittance-based measured methods (C–V and G/w–V). As seen in Fig. 4, the series resistance gives a peak between about 0–1 V depending on frequency and disappears at sufficiently high frequencies.

From Fig. 4 it is clearly seen that the series resistance is dependent both frequency and voltage and changes from region to region. These behaviors considered that the trap charges have enough energy to escape from the traps located at metal/semiconductor interface in the Si band gap. Also the obtained R_s–f at various forward biases is given Fig. 5. It is clear seen in Fig. 5, that the R_s is independent of voltage at sufficiently high frequency ($f \geqslant 1$ MHz).

In order to clarify the observed behavior of C_m and G_m/w in Fig. 3a and b, we have measured the C_m and G_m/w of Al–TiW–Pd_2Si/n-Si structure as a function of frequency at the fix gate voltage (Fig. 6). From this figure, it is visible that the changes of the C_m and G_m/w take place over a wide frequency range. The conductance peaks, of which the frequency position depends on the gate voltage, occur

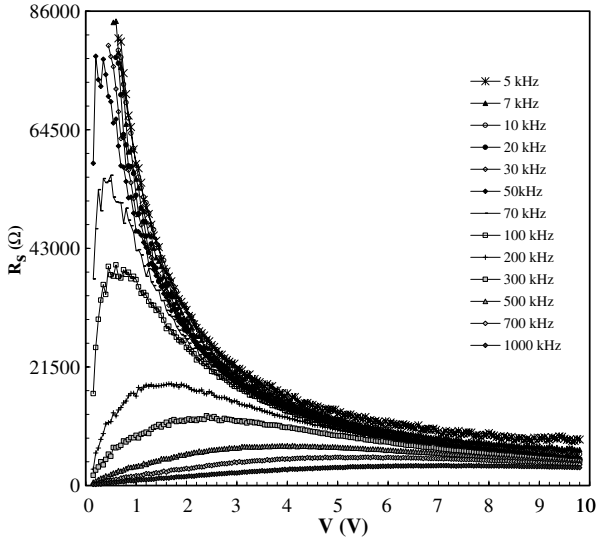

Fig. 4. The R_s–V plots at various frequencies for Al–TiW–Pd_2Si/n-Si structure at room temperature.

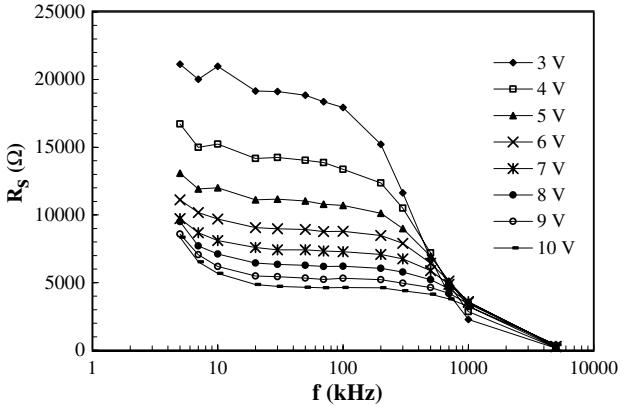

Fig. 5. The variation of R_s as a function of frequency for Al–TiW–Pd_2Si/n-Si structure at room temperature.

and the capacitance dispersion exists in frequency range where G_m/w maxima are observed. The results indicate the presence of the low frequency dispersion of the capacitance and conductance for the investigated structure. Such frequency dependence are observed in the literature [13–15,29–31].

According to high-low frequency capacitance method, the interface states density N_{ss} can be extracted from its capacitance contribution to the measured C–V curve [7,32]. In the equivalent circuit of the structure, the insulator capacitance C_{ox} is in series with the parallel combination of the interface state capacitance C_{ss} and the space charge capacitance C_{sc}. Because N_{ss} do not follow high frequencies in inversion and depletion region, the measured high frequency capacitance (C_{HF}) in this region do not contain interface states capacitance. The interface state capacitance can be determined by subtracting the depletion layer capacitance from the depletion layer capacitance in parallel with interface states capacitance. Thus the density of interface state profile is calculated from Eq. (7) and given in Fig. 7.

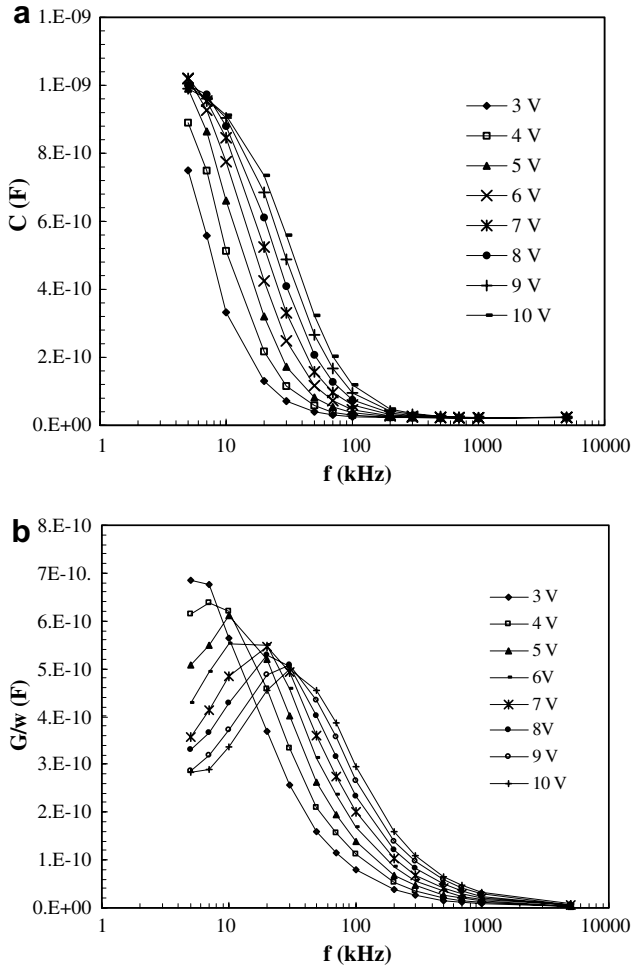

Fig. 6. The frequency dependence of (a) the $C(V_G)$–f and (b) $G/\omega(V_G)$–f characteristics of the Al–TiW–Pd_2Si/n-Si structure at room temperature.

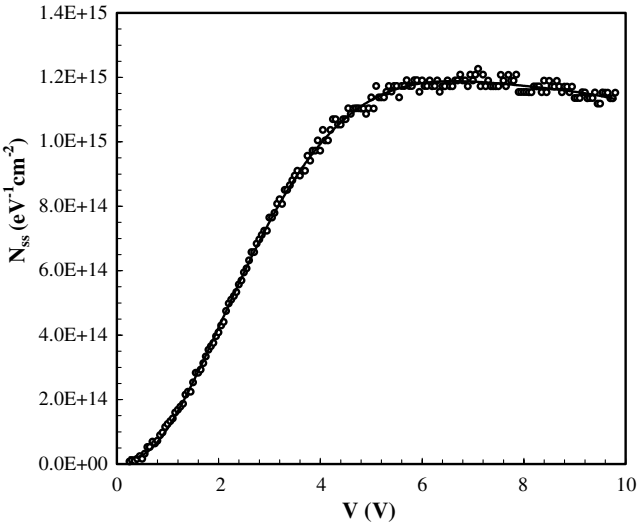

Fig. 7. The energy distribution profile of the N_{ss} obtained from high-low frequency capacitance technique for Al–TiW–Pd_2Si/n-Si structure at room temperature.

$$qAN_{ss} = C_{SS} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - \left[\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right]^{-1} \quad (7)$$

where A is the area of rectifier contact and q is the electronic charge. The values of N_{ss} are of order about $10^{14}\,eV^{-1}\,cm^{-2}$, which is high enough to pin Fermi level of the Si substrate surface [33]. Despite the fact that it is seemed the disagreement in the N_{ss} profile between Figs. 2 and 7, there is a good agreement in N_{ss} especially at low voltage region (0–1.5 V).

4. Conclusion

The forward and reverse bias (C–V–f) and (G/w–V–f) characteristics of the Al–TiW–Pd_2Si/n-Si diodes carried out at room temperature. The C–V and G/w–V curves of the investigated structure at various biases between −4 V and 10 V show additional response which is independent of bias at high frequencies. The other explanation of the better response at lower frequencies may be due to balanced communication of interface traps with the valance and conduction bands of the Si substrate. This response is attributed to the surface states can easily follow the ac signal at low frequencies and yield an excess capacitance, which depends on the relaxation time of the surface states and the frequency of ac signal. The series resistance profile of Al–TiW–Pd_2Si/n-Si diode has been obtained from admittance measurements. The density of N_{ss} distribution profiles as a function of energy (E_c–E_{ss}) obtained from the I–V data by taking into account the bias dependence of the n and Φ_e. The N_{ss} show an exponential growth from midgap towards the bottom of the conductance band E_c. It can be concluded that the values of R_s are significant only in the downward curvature of the forward bias I–V and C–V characteristics at high bias voltage, but the values of N_{ss} are significant in both the low and high bias voltages. In conclusion, the ignoring the interface state density (N_{ss}) and series resistance (R_s) of device can lead to significant errors in the capacitance–voltage (C–V) and conductance–voltage (G/w–V) characteristics.

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