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The C–V–f and G/ω–V–f characteristics of Au/SiO_2/n-Si capacitors

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Abstract

Au/SiO_2/n-Si metal–insulator-semiconductor (MOS) structures with thermal growth oxide layer have been fabricated. The frequency dependence of capacitance–voltage (C–V) and conductance–voltage (G/ω–V) characteristics of these structures have been investigated taking into account the effect of the series resistance and interface states. The C–V and G/ω–V measurements have been carried out in the frequency range of 1 kHz–1 MHz at room temperature. The frequency dispersion in capacitance and conductance can be interpreted in terms of the interface states density (N_{ss}) and series resistance values (R_s). The interface states can follow the ac signal and yield an excess capacitance especially at low frequencies. The values of measured C and G/ω decrease in depletion region with increasing frequencies especially in low frequencies due to a continuous density distribution of interface states. The C–V plots exhibit anomalous peaks due to the N_{ss} and R_s effect. It has been experimentally found that the peak positions in the C–V plot shift towards positive voltages and the peak value of the capacitance decreases with increasing frequency. The effect of series resistance on the capacitance is found appreciable at high frequencies due to the interface state capacitance decreasing with increasing frequency. In addition, the high-frequency capacitance (C_m) and conductance (G_m/ω) values measured under both reverse and forward bias were corrected for the effect of series resistance to obtain the real diode capacitance. Experimental results show that the locations of interface states between Si/SiO_2 and series resistance have a significant effect on electrical characteristics of MOS structures.

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Keywords: MOS structure; Frequency dependence; Series resistance; Interface states

1. Introduction

The metal–insulator-semiconductor (MOS) structures consist of a semiconductor substrate covered by an oxide layer with thickness of between 50 and 5000 Å and metal. The presence of an insulator layer between metal and semiconductor in the MOS structure gives these devices the properties of a capacitor, which stores the electric charge by virtue of the dielectric property of oxide layers. Due to the existence of oxide layer and two surface-charge regions, MOS physics is more complicated than semiconductor surface physics. The important role of these structures in Si technology, the semiconductor/insulator (Si/SiO_2) interface and defects on its neighborhood have been extensively studied in the past four decades [1–16].

The interface states density (N_{ss}) and series resistance values (R_s) of a metal-semiconductor the MOS structures are important parameters that affect their main electrical parameters [3,7,17,18]. When a voltage is applied across the MOS diode, the combination of the interfacial insulator layer, depletion layer and the series resistance of the device will share applied voltage. There are several suggested methods [19–23], which could help to determination of the R_s, and among them the more important is the conductance technique developed by Nicollian and Goetzberger [3]. In MOS structure metal and semiconductor remain separated by an insulating layer and there is a continuous distribution of interface states at semiconductor/insulator interface. The forward and reverse bias C–f and G/ω–f measurements give the important information about the

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energy distribution of the interface states of the MOS structure. At high frequencies, $f \geqslant 500$ kHz (such the carrier life time τ is much larger than $1/\omega$), the charges at the interface states cannot follow an AC signal. In contrary, at low frequencies, about 50 Hz, the charges can easily follow an ac signal and they are capable of these charges increase with decreasing frequency. Therefore, the frequency dependent electrical characteristics are very important according to accuracy and reliable results. The characterization of interface states in MOS structure has become a subject of very intensive research in the last decade, and a number of workers have suggested various ways of characterization [12,15,17,24–26]. In order to achieve a better understanding of the effects of different charge interface states and series resistance, we measured the capacitance (C) and conductance (G/ω) as a function of applied voltage at wide range of frequency. In general, the C–f and G/ω–f curves in the ideal case are frequency independent and C–V plot shows an increase in capacitance with an increase in forward bias [8,22,23,27]. However, in ideal case this is often disturbed due to the presence of interfacial insulator layer between the metal-semiconductor interface and series resistance of MOS structure [1,25,27].

In this paper, we investigate the effects of the series resistance and interface states, which cause non-ideal behavior on electrical characteristics of MOS structure and we report results of a systematic investigation on the frequency dependence of the electrical properties of MOS structure. To do this, the electrical properties of MOS structure were investigated in the frequency range of 1 kHz–1 MHz at room temperature. Also, to obtain the real MOS capacitance without the effect of R_s, the high-frequency C and G/ω measurements under both reverse and forward bias (from −4 to 6 V) were corrected.

2. Experimental procedure

The Au/SiO_2/n-Si MOS structure was fabricated on a quarter of 2″ diameter float zone ⟨1 0 0⟩ n-type (phosphor doped) single crystal silicon (Si) wafer having thickness of 350 μm with 0.8 Ω-cm resistivity. For the fabrication process the Si wafer was degreased in organic solutions of $CHCICCI_2$, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 an H_2O_2 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally quenched in de-ionized water for a prolonged time. Preceding each step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ-cm. The high purity gold with a thickness of ≈2000 Å was thermally evaporated from tungsten filament onto the whole back side on the n-Si wafer at a pressure of $\approx 1 \times 10^{-6}$ Torr in liquid nitrogen trapped oil-free ultra high vacuum pump system. The ohmic contact was formed by sintering the evaporated Au back contact at 750 °C for 95 min in a flowing dry oxygen ambient at rate of 1 lt/min. This process served both to sinter the Au and to form the required thin interfacial oxide layer (SiO_2) on the upper surface of the n-Si wafer. After oxidation, circular dots of 1 mm diameter and 2000 Å thick gold contacts were deposited onto the oxidized surface of the wafer through a metal shadow mask in a liquid nitrogen trapped vacuum system in a vacuum of $\approx 1 \times 10^{-6}$ Torr.

The C–V and G/ω–V measurements were performed in the frequency range of 1 kHz–1 MHz by using a HP 4192A LF impedance analyser and small sinusoidal test signal of 40 mV_{p-p} from the external pulse generator was applied to the sample in order to meet the requirement [3]. All measurements were carried out with the help of a microcomputer through an IEEE-488 AC/DC converter card.

3. Results and discussions

The conductance technique [5,14,28] is based on the conductance losses resulting from the exchange of majority carriers between the interface states and majority carrier band of the semiconductor when a small ac signal is applied to the MOS structures. The applied ac signal causes the Fermi level to oscillate about the mean positions governed by the DC bias, when the MOS structure is in the depletion. In Nicollian and Goetzberger's statically theory [3,27], the random distribution of discrete insulator charges and charged interface states in the semiconductor/insulator (Si/SiO_2) interface plane cause a non-uniform distribution of surface band bending over the interfacial plane.

To extract the series resistance of MOS structure, several methods have been suggested [10–12]. In this study, we have been used the conductance method developed by Nicollian and Goetzberger [3,27]. The C–V and G/ω–V characteristics of Au/SiO_2/n-Si MOS structure were measured in the frequency range of 1 kHz–1 MHz. The real series resistance of MOS structures can be subtracted from the measured capacitance (C_{ma}) and conductance (G_{ma}) in strong accumulation region at high frequency ($f \geqslant 500$ kHz) [14,23,27]. In addition, the voltage and frequency dependence of the series resistance profile can be obtained from the C–V and G/ω–V curves. To determine series resistance R_s, the MOS structure is biased into strong accumulation at sufficiently high frequency. The measured admittance (Y_{ma}) at strong accumulation of MOS structure using the parallel RC circuit [22,23] is equivalent to the total circuit impedance as

$$Y_{ma} = 1/Z_{ma} = (G_{ma} + j\omega C_{ma}). \quad (1)$$

Comparing the real and imaginary part of the impedance, the series resistance is given by [19,23]

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2}, \quad (2)$$

where C_{ma} and G_{ma} represent the measured capacitance and conductance in strong accumulation region. The capacitance of insulator oxide layer C_{ox} is related to series

resistance by

$$C_{ma} = \frac{C_{ox}}{(1 + \omega^2 R_s^2 C_{ox}^2)}. \quad (3)$$

From this relation, C_{ox} is obtained as

$$C_{ox} = C_{ma}\left[1 + \left(\frac{G_{ma}}{\omega C_{ma}}\right)^2\right] = \frac{\varepsilon_i \varepsilon_o A}{d_{ox}}, \quad (4)$$

where $\varepsilon_i = 3.8\varepsilon_o$ [23] and ε_o are the permittivities of the interfacial insulator layer and free space.

Finally, by comparing the imaginary and real part of corrected admittance ($Y_c = 1/(G_c + j\omega C_c)$) one obtains the corrected capacitance (C_c) and conductance (G_c) as

$$C_c = \frac{[G_m^2 + (\omega C_m)^2]C_m}{a^2 + (\omega C_m)^2} \quad (5)$$

and

$$G_c = \frac{G_m^2 + (\omega C_m)^2 a}{a^2 + (\omega C_m)^2}, \quad (6)$$

where

$$a = G_m - [G_m^2 + (\omega C_m)^2]R_s. \quad (7)$$

The insulator layer thickness d_{ox} calculated for the MOS structure from high frequency ($f \geqslant 1$ MHz) C–V curve using the Eq. (4) was found to be 58 Å. The values of the capacitance and conductance depend on a number of parameters, such as series resistance, density of interface states and the formation of insulator layer between metal and semiconductor. The effect of density of interface states can be eliminated when the C–V and G/ω–V plots are obtained at sufficiently high frequency [22], since the interface states does not follow AC signal above this frequency. In this case, the series resistance seems the most important parameter, which causes the electrical characteristics of Au/SiO_2/n-Si MOS structures to be non-ideal [6,7,9,11].

The density of interface states (N_{ss}) can be derived from Hill–Coleman method [29]. According to this method, the density of interface states can be calculated by using the following equation:

$$N_{ss} = \frac{2}{qA}\frac{(G_m/\omega)_{max}}{((G_m/\omega)_{max}C_{ox})^2 + (1 - C_m/C_{ox})^2)}, \quad (8)$$

where A is the area of the diode, ω the angular frequency, and $(G_m/\omega)_{max}$ the maximum measured conductance value. C_{ox} is the capacitance of insulator layer in strong accumulation region and C_m is the capacitance value, which corresponding to the $(G_m/\omega)_{max}$ value.

Fig. 1 shows the experimental C–V and G/ω–V curves of the Au/SiO_2/n-Si MOS structure, respectively, in the frequency range from 50 kHz to 1 MHz at room temperature. As can be seen Figs. 1(a) and (b), the low-frequency capacitance and conductance changes with applied voltage while the high-frequency capacitance remains almost constant. In other words, in the high frequency, the N_{ss}

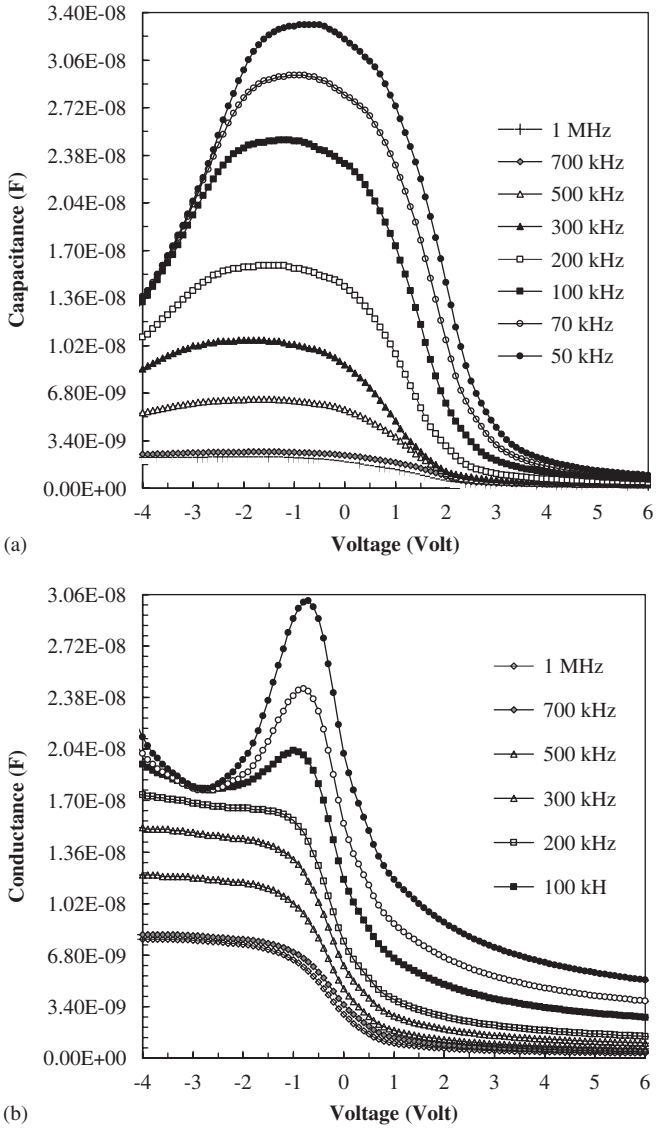

Fig. 1. The frequency dependent plot of (a) the C–V and (b) G/ω–V characteristics of the Au/SiO_2/n-Si MOS structure at room temperature.

cannot follow the AC signal and consequently do not contribute appreciably to the MOS capacitance.

This situation may be different at low and intermediate frequencies, depending on the relaxation time and of N_{ss} and the frequency of the ac signal [3].

The other explanation of this behavior of C–V and G/ω–V characteristics can be made by whether the interface state charges contribute to the MOS capacitance and conductance or the charge at interface states can follow an alternating current signal. As a result we can say that in the low frequencies N_{ss} can follow the ac signal and yield an excess capacitance, which depends on the frequency, but in the high frequency limit ($f \geqslant 500$ kHz), the interface states cannot follow the ac signal. This makes the contribution of interface state capacitance to the total capacitance negligibly small [18,23].

As shown from Figs. 1(a) and (b), both C–V and G/ω–V curves have three regimes of accumulation-depletion-

inversion region. Especially, in the depletion region for a given applied voltage the value of capacitance increases with decreasing frequency due to the time dependent response of interface states. In the inversion region of especially C–V curves no appreciable frequency dispersion is evident in this frequency range. Also, C–V and G/ω–V curves at low frequencies give a peak in the depletion region. Such behavior of the C and G/ω peaks are attributed to particular distribution of surface states between Si/SiO_2 interface. From the above discussion it can be concluded that under bias (V) the interface states are responsible for the observed frequency dispersion in C–V and G/ω–V curves. Therefore, depending on the relaxation time of the interface states and the frequency of the ac signal, there may be a capacitance due to interface states in excess to depletion layer capacitance. The N_{ss} calculated from Eq. (8) as a function of frequencies are shown in Fig. 2(a). As seen in Fig. 2(a), The N_{ss} values decrease with decreasing frequencies. On the other hand, the values of N_{ss} was estimated using the combination of low frequency (C_{LF}) and high frequency (C_{HF}) method to the following equation [23]:

$$N_{ss} = q/A\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right], \qquad (9)$$

where C_{LF} is the lowest value of the low frequency (1 kHz) capacitance, C_{HF} is the high frequency (500 kHz) capacitance at voltage corresponding to C_{LF}, C_{ox} is the accumulation insulator layer capacitance, and A is the capacitance area. The results are presented in Fig. 2(b). The values of N_{ss} are of order $10^{13}\,eV^{-1}\,cm^{-2}$ which are closer to the values of obtained I–V measurements.

Figs. 3(a) and (b) show the capacitance (C) and conductance (G/ω) in depletion region as a function of frequency in the voltage range of (0) to (−2.4) V, with the step of 0.4 V as a parameter. As can be seen in Figs. 3(a) and (b), the measured C and G/ω in depletion region

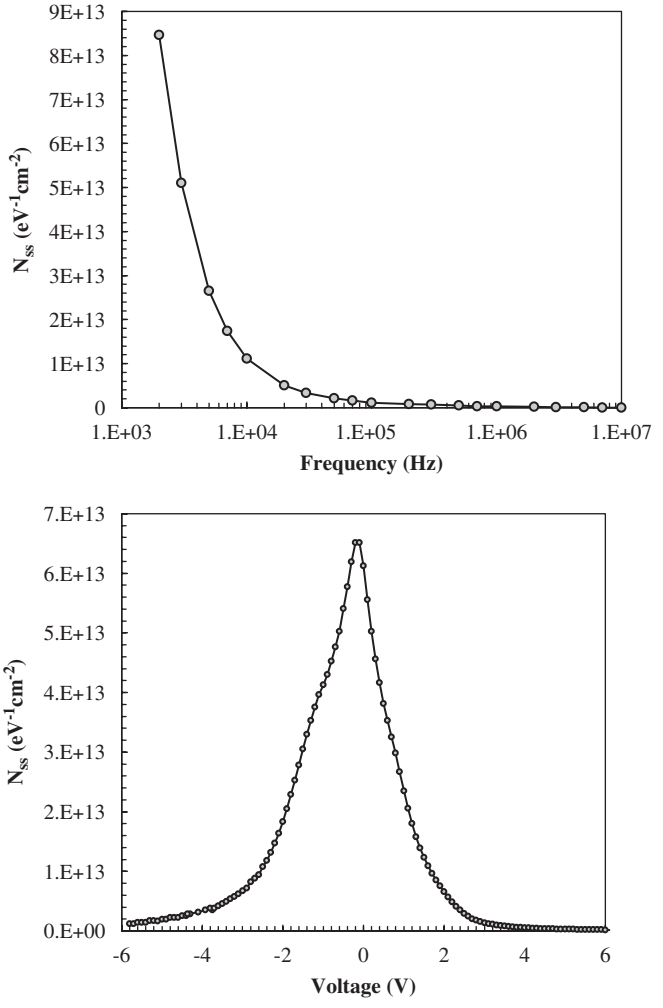

Fig. 2. (a) The variation of N_{ss} as a function of frequency for $Au/SiO_2/n$-Si MOS structure and (b) the variation of the N_{ss} as a function of voltage obtained from the C_{LF}–V and C_{HF}–V characteristics of the $Au/SiO_2/n$-Si MOS structure at room temperature.

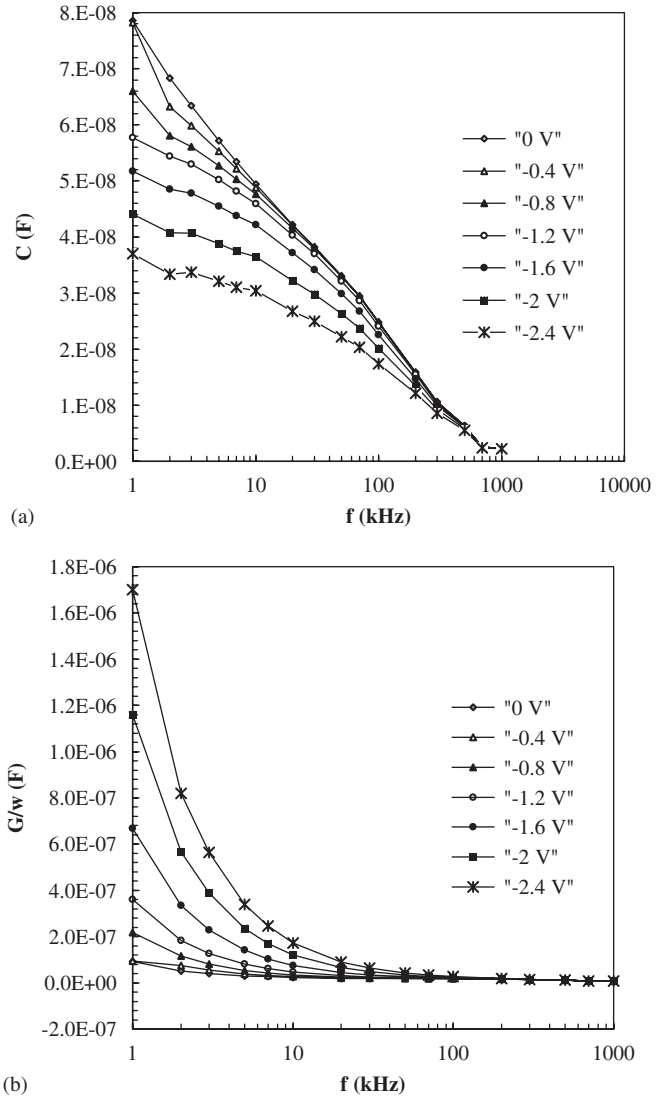

Fig. 3. The frequency dependence of (a) the $C(V_G)$–f and (b) $G/\omega(V_G)$–f characteristics of the $Au/SiO_2/p$-Si MIS structure for different reverse bias at room temperature.

decrease with increasing frequency in the frequency range of 1 kHz–1 MHz. This behavior is attributed to the presence of a continuous distribution of N_{ss}, which leads to a progressive decrease of the response of the N_{ss} to the applied alternating-current voltage [5,18,22–25,27].

In addition, the higher values of C and G/ω at low frequency are due to excess capacitance and conductance resulting from the N_{ss} in equilibrium with the semiconductor that can follow the ac signal. It can be concluded that under reverse bias the interface states are responsible for the observed frequency dispersion in $C(V_G)$ and $G/\omega(V_G)$ curves.

The series resistance of MOS structure is calculated according to Eq. (2) and shown in Fig. 3 for various frequencies, and the frequency dependence of R_s for different reverse bias at room temperature is plotted in Fig. 4. These very significant values demanded that special attention be given to effects of the series resistance in the application of the admittance-based measured methods (C–V and G/ω–V).

As seen in Fig. 4, the series resistance gives a peak at low frequency in the voltage range about (−1.25) to (−2.25) V range. From Fig. 5, it is clearly seen that the voltage dependent series resistance remained almost constant up to 500 kHz. We considered that the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the Si band gap. Also, at high frequencies, $f \geqslant 500$ kHz, the charges at the interface states cannot follow an ac signal [13,23,27].

As can be seen in Figs. 1 and 2, both in the depletion and accumulation region measured C and G/ω were highly dependent on frequency. Therefore, to obtain the real diode capacitance C_c and conductance G_c/ω, the high frequency capacitance measured under forward and reverse bias was corrected for the effect of series resistance using Eqs. (5) and (6), respectively. When the correction was made on the C–V and G/ω plots for the effect of series resistance, the values of the corrected capacitance C_c and conductance G_c/ω changes, especially under reverse bias, as in Fig. 6(a) and (b), respectively.

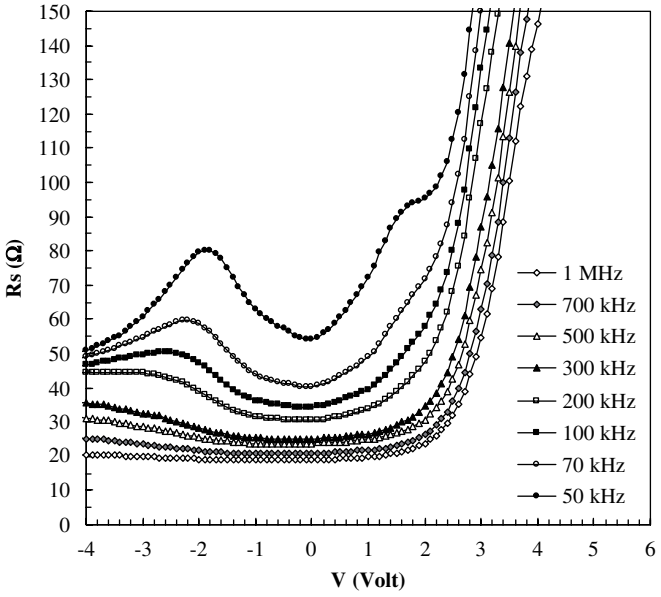

Fig. 4. The variation of the series resistance as a function of voltage for various frequencies at room temperature.

4. Conclusion

The forward and reverse bias C–V and G/ω–V characteristics of the Au/SiO_2/p-Si MOS structure were measured in the frequency range of 1 kHz–1 MHz at room temperature. The ultrathin (58 Å) SiO_2 interfacial insulator layer between metal and semiconductor was grown on silicon (Si) substrate with thermally oxidation. The peak values of C–V and G/ω–V especially at low frequencies have been found to be strongly dependent on the values of interface state density (N_{ss}) and series resistance (R_s). The

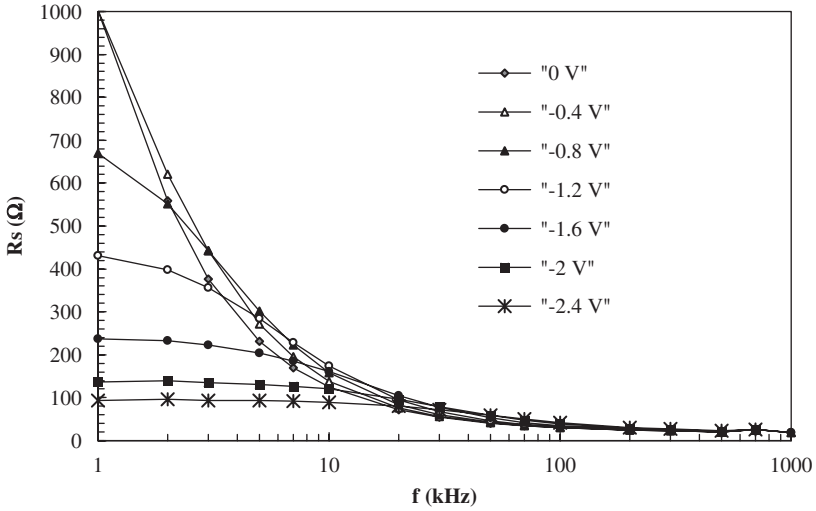

Fig. 5. The frequency dependence of the series resistance for different reverse bias at room temperature.

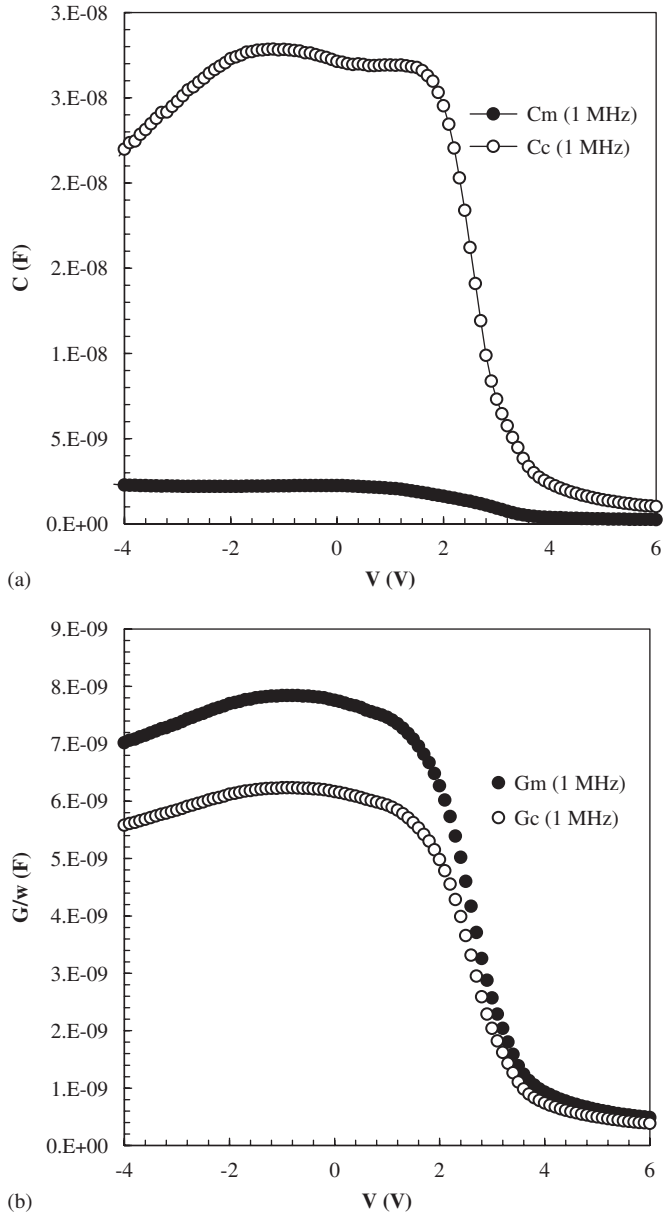

Fig. 6. The voltage dependent plots of the corrected (a) the high frequency (1 MHz) capacitance and (b) conductance curves at room temperature.

experimental results confirmed that both the measured C and G/ω varies with applied voltage and frequency, and decreases with increasing frequency in depletion and accumulation region due to a continuous distribution of interface states between Si/SiO_2 interface. Also, it can be explained that the N_{ss} can follow the ac signal and yield an excess capacitance and conductance, which depends on the relaxation time of N_{ss} and frequency of the applied ac signal. It was found that the measured C–V and G/ω–V characteristics in the depletion and accumulation regions were highly dependent on frequency. Therefore, measured C–V and G/ω–V data at high frequencies were corrected for the effect of series resistance.

The C–V and G/ω–V characteristics confirm that the R_s and N_{ss} are important parameters that strongly influence the electric parameters in MOS structure.

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