Available online at www.sciencedirect.com
ScienceDirect
Physica B 388 (2007) 10–15
PHYSICA B
www.elsevier.com/locate/physb

The effect of series resistance and oxide layer formed by thermal oxidation on some electrical parameters of Al/SiO_2/p-Si Schottky diodes

İlbilge Dökme

Science Education Department, Faculty of Education, Ahi Evran University, Kırşehir, Turkey

Received 10 April 2006; received in revised form 26 April 2006; accepted 27 April 2006

Abstract

Two types of Schottky diodes with and without thermal-growth oxide layer, were fabricated to investigate whether or not the thermal-growth oxide layer is effective on some electrical parameters such as ideality factor n, barrier height Φ_B, series resistance R_s and interface state density N_{ss}. The current–voltage (I–V) characteristics were measured for these two diodes at 150 K and room temperature (300 K). Electrical parameters of these two diodes were calculated and compared at two temperatures. At the temperatures of 150 and 300 K, Φ_B, n, and R_s for diode without oxide layer ranged from 0.50 to 0.81 eV, 4.12 to 1.54, and 481 to 156 Ω respectively. The Φ_B, n, and R_s for diode with thermal-growth oxide layer have ranged from 0.54 to 0.87 eV, 6.83 to 1.66, and 503 to 281 Ω, respectively. For two diodes, the temperature dependence energy density distribution profiles of interface state were obtained from forward bias I–V measurements by taking into account the bias dependence of effective barrier height Φ_e and R_s of the devices and the value of N_{ss} in diode without oxide layer is almost one order of magnitude larger than the diode with oxide layer.
© 2006 Elsevier B.V. All rights reserved.

PACS: 73.20.−r; 73.30.+y; 73.40.Qv

Keywords: Schottky diodes; MS structure; MIS structure; Thermal oxidation; Insulator layer; Interface states

1. Introduction

The surface stability of semiconductors plays a very important role in the fabrication of electronic devices such as metal–semiconductor (MS) or metal–insulator–semiconductor (MIS) Schottky diodes. These types of devices have been gaining importance due to a wide variety of optoelectronic and high-frequency applications. The performance and reliability of these devices especially depend on the density of interface states, series resistance and interfacial insulator layer between metal and semiconductor. The existence of an insulating oxide layer at the MS interface coverts the device into a MIS diode [1–5]. An insulator layer on Si to fabrication MIS Schottky diodes is formed by ways of oxidation, deposition or surface passivation. However, during fabrication process of MS diodes, an oxide layer can be formed on semiconductor by natural ways. The semiconductor is covered with thin oxide layer, either during sample preparation, metal evaporation, when carried out in a conventional vacuum system, or thermal annealing [6–9]. The presence of a thin oxide layer may cause an interface state charge with bias due to an additional field in the interfacial layer and influence the diode electrical characteristics [6,10–12]. Therefore, the interfacial parameters such as the interface state density and the thickness of the interfacial oxide layer give rise to masking of the real electrical characteristics of the Schottky diodes [1,2,10,13,14]. Another effect on the I–V characteristics of Schottky diode is when the diode has a series resistance, associated with the semiconductor bulk which causes voltage drop across the junction to be less than the applied voltage between the terminals of the diode. For the case of a diode with a high series resistance, I–V characteristics of Schottky diode are different from the expected, especially high forward bias region [1,3,10,15–17].

The first studies on the interfacial insulator layer between metal and semiconductor in Schottky diodes were

E-mail address: ilbilgedokme@gazi.edu.tr.

0921-4526/$ - see front matter © 2006 Elsevier B.V. All rights reserved.
doi:10.1016/j.physb.2006.04.032

made by Cowley and Sze [3], who obtained their estimations from an analysis of the Schottky barrier heights with different metallization as a function of metal work function. Card and Rhoderick [5], Horvath [18] and Tseng and Wu [4] estimated the interface state density located at the oxide silicon interface and examined effects of the interface states on the ideality factor of the forward-bias I–V characteristics. Some studies [4,5,13,19–23] inspected the effects of the presence of an interfacial oxide layer and the interface states on the behaviour of Schottky diodes, and extracted the density distribution of interface states in the semiconductor band gap from the forward-bias I–V characteristics. Different experimental techniques such as the ballistic electron emission and spectroscopy were used by some investigators to understand the Schottky barrier formation mechanism and electron properties of interface [24–29]. Aydın et al. [6] explained the importance of the fact that the neutral-region resistance value is considered in calculating the interface state density distribution from the non-ideal forward-bias I–V characteristics. Moreover, Kılıçoğlu and Asubay [30] research the effect of native oxide layer on some electronic parameter of Au/n-Si/Au-Sb Schottky diode.

In this work, the effect of thermal-growth oxide layer on some electronic parameter of Schottky diodes has been researched. Schottky diodes with and without thermal-growth oxide layer have been fabricated. The aim of this study is to compare some electronic parameters of these diodes and investigate the effect of thermal growth oxide layer on device parameters. For testing the finding at room temperature, I–V characteristics of these diodes were measured at 150 K and the influences of thermal-growth oxide layer on the forward-bias I–V characteristic were also examined at 150 K. In addition, the importance of calculating the interface states density distribution from the non-ideal I–V characteristics of the Schottky diodes, taking into account series resistance contribution is presented.

2. Experimental procedure

Samples have been prepared using p-type (boron-doped) single-crystal silicon wafer with $\langle 100 \rangle$ orientation, thickness of 350 μm and $\approx 2\,\Omega$ cm resistivity. For the fabrication process the Si wafer was degreased in organic solutions of $CHCICCI_2$, CH_3COCH_3 and CH_3OH, then etched in a sequence of H_2SO_4 and H_2O_2 20% HF, a solution of $6HNO_3$:1HF:$35H_2O$, 20% HF and finally quenched in de-ionized water for a prolonged time. Preceding each step, the wafer was rinsed thoroughly in de-ionized water of resistivity of 18 MΩ cm. The wafer was cut into two pieces and named D1 and D2.

For fabricating D1, the aluminium (Al) back contact was thermally evaporated by means of a tungsten filament onto the whole back of silicon crystal under a pressure of 1×10^{-6} Torr. The low resistivity ohmic back contact to p-type Si wafers was made by using high purity Al (99.999%), and followed by a temperature treatment at 550 °C for 5 min in dry nitrogen N_2 atmosphere. Then, D-MS was inserted into the evaporation chamber for forming the rectifier contact. The rectifier contacts were formed onto front face of Si by evaporation of high purity Al dotes with diameter of about 1 mm.

For fabricating D2, however, the high-purity Al was thermally evaporated from tungsten filament onto the whole back side on the p-Si wafer at a pressure of $\approx 1 \times 10^{-6}$ Torr in liquid nitrogen-trapped oil-free ultra high vacuum pump system. The ohmic contact was formed by sintering the evaporated Al back contact at 700 °C for 60 min in a flowing dry oxygen ambient at rate of 1 l/min. This process served both to sinter Al and to form the required thin interfacial oxide layer (SiO_2) on the upper surface of the p-Si wafer. After thermal oxidation, circular dots of 1 mm diameter and 2000 Å thick Al contacts were deposited onto the oxidized surface of the wafer through a metal shadow mask in liquid nitrogen trapped vacuum system in a vacuum of $\approx 1 \times 10^{-6}$ Torr. The interfacial oxide layer thickness was estimated to be about 40 Å from measurement of the oxide capacitance at the strong accumulation region for MIS structure [31].

The forward-bias I–V measurements were performed by the use of a Keithley 220 programmable constant-current source, a Keithley 614 electrometer at room temperature. The C–V measurements were performed by using a HP 4192A LF impedance analyser at 1 MHz and small sinusoidal test signal of 40 mV_{p-p} from the external pulse generator was applied to the sample in order to meet the requirement. In addition, all measurements were performed at 150 K by the use of a temperature-controlled Janes vpf-475 cryostat.

3. Results and discussion

For a MS or MIS Schottky diode with series resistance, it is assumed that the net current of the device is due to thermionic emission theory and it can be expressed as [1,2,15,16,32]

$$I = I_0\left[\exp\frac{q}{nkT}(V - IR_s)\right], \tag{1a}$$

where V is the definite forward-bias voltage, IR_s the voltage drop across series resistance of the device, n the ideality factor, k the Boltzmann constant, and T temperature in Kelvin and I_0 the reverse saturation current expressed as

$$I_0 = A^* A\, T^2 \exp(-q\Phi_B/kT), \tag{1b}$$

where the quantities A^* A, Φ_B are the effective Richardson constant and (equal to 32 A/cm^2K^2 for p-type Si), the diode area and, the zero-bias barrier height, respectively.

Ideality factor is a measure of conformity of the diode to pure thermionic emission and is contained in the slope of straight-line region of the forward-bias logarithmic

characteristics of I–V through the relation

$$n = \frac{q}{kT}\left[\mathrm{d}(V)/\mathrm{dL}n(I)\right]. \quad (2)$$

Fig. 1 shows the experimental I–V characteristics of samples D1 and D2. The Φ_B and n values of these samples were calculated with the help of Eqs. (1b) and (2) from the y-exis intercept and slope of the linear region of the semi-log forward-bias I–V plots, respectively. At the temperatures of 300 K and 150 K, the values of n are 1.54 and 4.12 for the sample D1 and 1.66 and 6.83 for the sample D2, respectively. Barrier height of the sample D1 and D2 were found to be 0.81 and 0.87 eV (at 300 K), and 0.50, 0.54 eV (at 150 K), respectively.

In general, the forward-bias I–V characteristic is linear on a semilogarithmic scale at low forward-bias voltages but deviates considerably from linearity due to the effect of series resistance R_s, the interfacial layer, and the interface states when the applied voltage is sufficiently large. The series resistance is important in the downward curvature of the forward-bias I–V characteristics, while the other two parameters are important in both linear and non-linear regions of I–V characteristics. Therefore n, Φ_B and R_s were evaluated using a method developed by Cheung and Cheung [16] in the high-current range where the I–V characteristic is not linear. According to this method from Eq. (1a), the following functions can be written

$$\frac{\mathrm{d}V}{\mathrm{d}\ln I} = n\frac{kT}{q} + IR_s, \quad (3)$$

$$H(I) = V + n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right), \quad (4)$$

and $H(I)$ is given as

$$H(I) = n\Phi_B + IR_s. \quad (5)$$

Eq. (3) should give a straight line for the data of downward-curvature region in the forward-bias I–V characteristic. Thus, a plot of $\mathrm{d}V/\mathrm{d}(\ln I)$ vs. I will give R_s as the slope and nkT/q as the y-axis intercept. Using the n value determined from Eq. (3) and the data of downward curvature region in Eq. (4), a plot of $H(I)$ vs. I according to Eq. (5) will also give a straight line with y-axis intercept equal to $n\,\Phi_B$. From $\mathrm{d}V/\mathrm{d}(\ln I)$ vs. I plot by means of Eq. (3), the values of R_s and n of sample D1 and D2 are given in Table 1. The values of Φ_B and R_s from $H(I)$–I plot according to Eq. (5) are also seen in this table.

As seen in Table 1, the values of n calculated from thermionic emission theory are poorer than those calculated from Cheung function. At two temperatures the n values of the sample D1 has been found to be smaller than those of the sample D2. However, the ideality factor value of 1.36 for the sample D1 at room temperature is high for ideal MS Schottky diode. This can be attributed to the presence of native oxide layer which may form on silicon by natural ways. For the sample D1, the native interface oxide layer may form during surface preparation or metal evaporation [1,2,6,33]. The silicon surface is inevitably covered with a native thin oxide layer whose thickness is between 10 and 30 Å, if the silicon surface is prepared by the usual polishing and chemical etching, and the evaporation of metal is carried out in a conventional vacuum system [1,6,9]. For a sufficiently thick interface insulator layer, the interface states are in equilibrium with the semiconductor, and they cannot interact with the metal [1,2,6,10]. That is to say, the studied samples behave MIS configuration with different interfacial oxide thicknesses. The high values of ideality factor at low temperature are ascribed interface states density and high series resistance. In the downward curvature region of forward-bias I–V plots of the samples D1 and D2 at sufficiently large

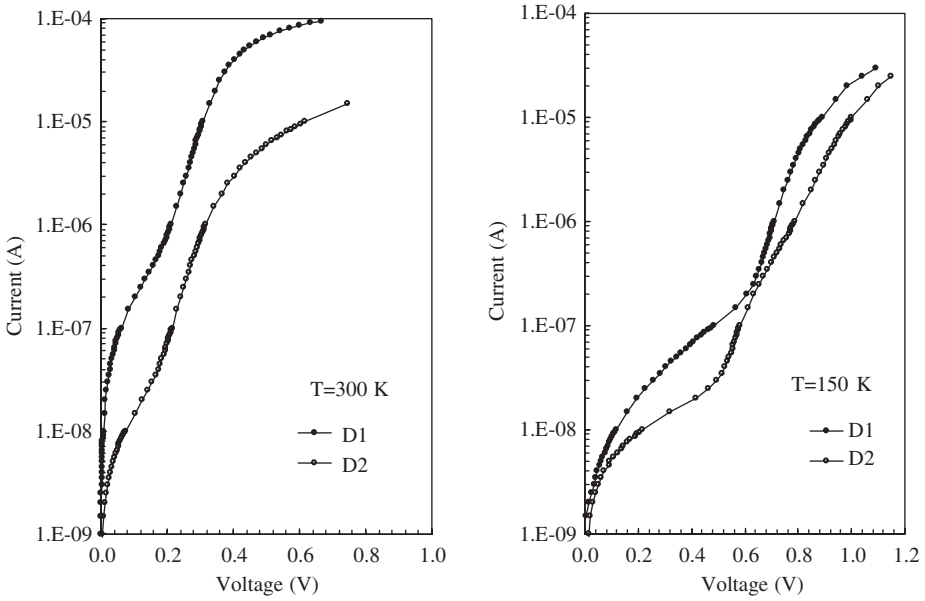

Fig. 1. The experimental forward-bias I–V characteristics of Schottky diodes with (D2) and without (D2) thermal growth oxide layer.

Table 1
The experimental values of some parameters obtained from I–V characteristics of the studied samples

T (K)	Sample	n (I–V)	n (dV/dLn I)	Φ_{Bo}(I–V)(eV)	Φ_{Bo}(H(I)(eV)	R_s(dV/dln I)(Ω)	R_s(H(I))(Ω)
300	D1	1.54	1.36	0.81	0.69	156	171
	D2	1.66	1.48	0.87	0.74	281	283
150	D1	4.12	4.12	0.50	0.42	481	484
	D2	6.83	6.70	0.54	0.48	503	508

voltages (Fig. 1), the ideality factor n is rather controlled by the interface states and series resistance.

The Φ_B values of the samples D1 and D2 were calculated as 0.81 and 0.86 eV at room temperature, respectively. A similar increase was also observed at 150 K. The barrier height value of D1 is lower than those of D2 because of additional potential drop across the interfacial layer. The higher interfacial oxide layer thickness is, the lower barrier height values then those of expected ideal Schottky barrier height.

As seen in Table 1, the obtained R_s values by different techniques are in good agreement with each other and the R_s values of the sample D1 has been found to be smaller than those of the sample D2. This can be attributed to the higher thickness of insulator oxide layer. The effect of the series resistance R_s is usually modelled with a series combination of a diode and a resistor with resistance R_s, through which the current I flows. When a forward bias V is applied across the device, the applied voltage V will be shared by the interfacial layer (V_i), the depletion layer (V_s) and the series resistance combination of the device R_s, and thus V can be written as

$$V = V_s + V_i + IR_s. \tag{6}$$

When the interfacial layer is sufficiently thick and the transmission probability between the metal and the interface states is very small, the effective barrier height Φ_e is assumed to be bias-dependent due to the presence of an interfacial insulator layer and interface states located between interfacial layer and semiconductor interface, and is given by [8,10,19]

$$\Phi_e = \Phi_B + \beta(V - IR_s) = \Phi_B + \left(1 - \frac{1}{n}\right)(V - IR_s), \tag{7}$$

where β is the voltage coefficient of the effective barrier height Φ_e used in place of the barrier height Φ_e [32–35] and for an MIS diode the ideality factor n becomes greater than unity as proposed by Card and Rhoderick [5].

$$n = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right], \tag{8}$$

where ε_s and ε_i are the permittivity of semiconductor and the interfacial layer, respectively, δ is the thickness of insulator layer, W_D the width of the space charge region and N_{ss} the density of the interface states in equilibrium with the semiconductor. Substituting the voltage dependence values of n and $\varepsilon_i = 3.8\varepsilon_o$, $\varepsilon_s = 11.8\varepsilon_o$ in Eq. (8), the

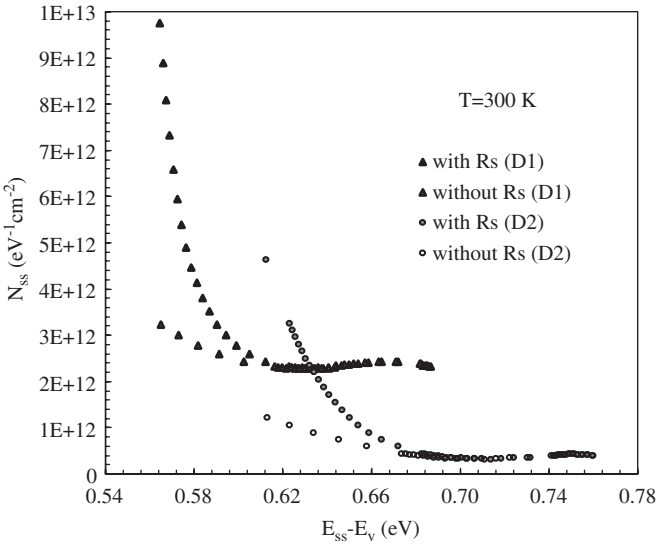

Fig. 2. The interface states energy distribution curves of the studied samples with and without taking into account the series resistance in the calculation at room temperature.

interface-states density distribution for the sample D1 and D2 were calculated by taking into account the contribution of the series resistance. The values of δ and W_D were calculated from capacitance and conductance measurements (1 MHz). The interfacial oxide layer thickness δ was obtained from high frequency (1 MHz) C–V characteristics using the equation for insulator layer capacitance ($C_{ox} = \varepsilon_i\varepsilon_o A/\delta$ where C_{ox} is the oxide capacitance in strong-accumulation region at 1 MHz and A is the diode area [2,22,31]. The values of δ and W_D were found to be about 33 Å and 3.5 μm for D1 and 42 Å and 4 μm for D2, respectively. The interfacial-layer thickness values δ (D1) = 33 Å for $n = 1.36$ and δ (D2) = 42 Å for $n = 1.48$ can usually cause the values of ideality factor greater than unity. [1].

In a p-type semiconductor, the energy of interface states N_{ss} with respect to the top of valance band E_v at the surface of the semiconductor is given by

$$E_{ss} - E_v = q(\Phi_e - V). \tag{9}$$

Fig. 2 shows the energy distribution profile of N_{ss} with and without taking into account R_s obtained from the forward-bias I–V characteristics of the fabricated samples at room temperature. As can be seen from Fig. 2, the exponential growth of N_{ss} from midgap towards the bottom of

conduction band is very apparent. The energy values of the density distribution of the interface states are in the range $0.56-E_v$ to $0.68-E_v$ eV and $0.61-E_v$ to $0.75-E_v$ eV, respectively. As can be seen in Fig. 2, the magnitude of the N_{ss} with and without taking into account the R_s in $0.56-E_v$ eV is 9.7×10^{12} and $3.2\times10^{12}\,eV^{-1}\,cm^{-2}$ for the sample D1, respectively. Also the magnitude of the N_{ss} is 4.6×10^{12} and $1.1\times10^{12}\,eV^{-1}\,cm^{-2}$, respectively, with and without taking into account R_s in $0.61-E_v$ eV for the sample D2. The N_{ss} values obtained taking into account the series resistance values are lower than those obtained without considering the series resistance.

After considering the series resistance value in the calculation related to the interface state density distribution, an exponential rise of the interface state density for the sample D1 from midgap towards the top of valence band is clearer than that of the interface state density for the sample D2 . This is attributed to the thermal oxidation on the cleaned Si surface of the sample D2. Furthermore, in the calculation made with and without considering the series resistance value of the devices, the N_{ss} value of the sample D1 is higher than that of the sample D2 in the same energy position (Fig. 2). A similar result is reported by Singh [36].

Fig. 3 shows the energy distribution profile of N_{ss} with and without taking into account R_s obtained from the forward-bias I–V characteristics of the fabricated samples at 150 K. The energy values of the density distribution of the interface states of D1 in the range $0.28\,E_v$ to $0.33-E_v$ eV are close to that of D2 in the range $0.28-E_v$ to $0.32-E_v$ eV. As can be seen in Fig. 3, the magnitudes of N_{ss} with and without taking into account R_s in $0.28-E_v$ eV are 2.5×10^{12} and $2.0\times10^{12}\,eV^{-1}\,cm^{-2}$ for the sample D1, respectively. Also the magnitudes of N_{ss} are 2.0×10^{12} and $1.9\times10^{12}\,eV^{-1}\,cm^{-2}$, respectively, with and without taking into account R_s in $0.28-E_v$ eV for the sample D2. As at the room temperature, the N_{ss} values obtained taking into account the series resistance values are lower than those obtained without considering the series resistance. After considering the series resistance value in the calculation related to the interface state density distribution, an exponential rise of the interface state density for the sample D1 from midgap towards the top of valence band is showing up sharply, while the interface state density for the sample D2 sample remains nearly unchanged.

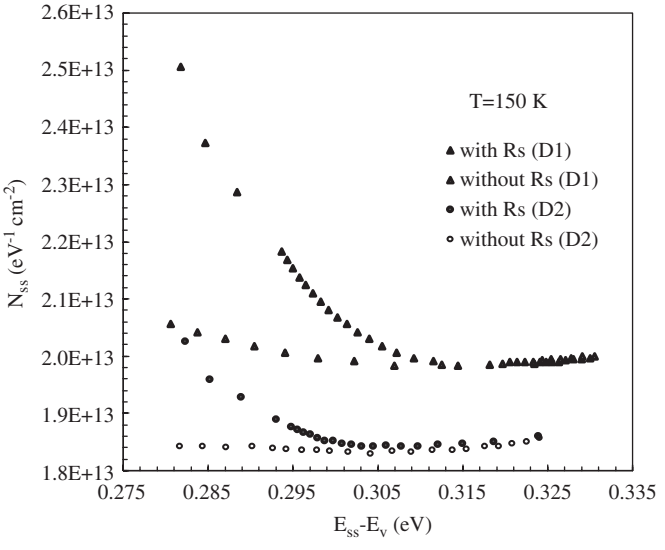

Fig. 3. The interface states energy distribution curves of the studied samples with and without taking into account the series resistance in the calculation at 150 K.

The profile of the density distribution curve of the interface states is in the range $0.56-E_v$ to $0.75-E_v$ eV at room temperature and $0.28-E_v$ to $0.33-E_v$ eV at 150 K. That is to say, the profile of the distribution of interface states density shifts to low voltage region at 150 K. As can be seen in Figs. 3 and 4, the values of N_{ss} are in the order of $\approx10^{12}\,cm^{-2}\,eV^{-1}$ at 300 K and $\approx10^{13}\,cm^{-2}\,eV^{-1}$ at 150 K. The effect of temperature on interface states is very apparent. The above explanation shows that the series resistance value should be taken into account in determining the interface state density distribution curves.

4. Conclusion

The semilogarithmic forward-bias I–V characteristics of Schottky diodes with and without thermal growth oxide layer were measured at 150 and 300 K. It is found that at the two temperatures n and R_s values of the Schottky diode with oxide layer are higher than those of diode without oxide layer while the Φ_B value of the Schottky diode with oxide layer is smaller than those of diode without oxide layer. The electrical parameters calculated from I–V characteristics of these samples indicated that both diodes have the MIS configuration. Al/p-Si with the ideality factor value of 1.36 at room temperature does not behave as an ideal Schottky diode because of the presence of native oxide layer which may form either during surface preparation or metal evaporation.

The interface states in equilibrium with the semiconductor were calculated from the downward-curvature region caused by the presence of R_s and interface states in the forward-bias I–V plots. As can be seen from the results, in order to obtain, as above, an accurate determination of the interface-state density distribution from the forward bias ln I–V characteristics, the series resistance value should be taken into consideration. It can be seen that the N_{ss} values, obtained by taking into account the series resistance value, are lower than those obtained without considering the series resistance.

References

[1] E.H. Rhoderick, R.H. Williams, Metal–Semiconductor Contacts, second ed., Clarendon Press, Oxford, 1988.
[2] S.M. Sze, Physics of Semiconductor Devices, second ed., Wiley, New York, 1981, p. 850.
[3] A.M. Cowley, S.M. Sze, J. Appl. Phys. 36 (1965) 3212.
[4] H.H. Tseng, C.Y. Wu, Solid State Electron 30 (1987) 383.

[5] H.C. Card., E.H. Rhoderick, J. Phys. D: Appl. Phys. 4 (1971) 1589.
[6] M.E. Aydın, K. Akkılıc, T. Kılıçoğlu, Physica B 352 (2004) 312.
[7] S. Zeyrek, Ş. Altındal, H. Yüzer, M.M. Bülbül, Appl. Surf. Sci. 252 (8) (2006) 2999.
[8] Ş. Altındal, İ. Dökme, M.M. Bülbül, N. Yalçın, T. Serin, Microelectron. Eng. 83 (3) (2006) 499.
[9] S. Özdemir, Ş. Altındal, Sol. Energy Mater. Sol. Cell 32 (1994) 115.
[10] P. Cova, A. Singh, A. Medina, R.A. Masut, Solid State Electron 42 (1998) 477.
[11] P.L. Hanselaer, W.H. Laflere, R.L. Van Meirhaeghe, F. Cardon, J. Appl. Phys. 56 (1984) 2309.
[12] H.H. Tseng, C.Y. Wu, Solid State Electron 30 (1987) 383.
[13] P. Chattopadhyay, A.N. Daw, Solid State Electron 29 (1986) 555.
[14] A. Türüt, M. Sağlam, Physica B 179 (1992) 285.
[15] H. Norde, J. Appl. Phys. 50 (7) (1979) 5052.
[16] S.K. Cheung, N.W. Cheung, Appl. Phys. Lett. 49 (1986) 85.
[17] Zs.J. Horvath, L. Dozsa, O.H. Krafcsik, T. Mohacsy, Gy. Vida, Appl. Surf. Sci. 234 (2004) 67.
[18] Z.S. Horvath, J. Appl. Phys. 63 (3) (1988) 976.
[19] A. Singh, K.C. Reinhardt, W.A. Anderson, J. Appl. Phys. 68 (7) (1990) 3475.
[20] P. Cova, A. Singh, Solid State Electron 33 (1) (1990) 11.
[21] B. Akkal, Z. Benemara, A. Boudissa, N.B. Bouiadjra, M. Amrani, L. Bideux, B. Gruzza, Mater. Sci. Eng. B 55 (1998) 162.
[22] Ş. Altındal, S. Karadeniz, N. Tuğluoğlu, A. Tataroğlu, Solid State Electron 47 (2003) 1847.
[23] Ş. Karataş, Ş. Altındal, M. Çakar, Physica B 357 (2005) 386.
[24] W.J. Kaiser, L.D. Bell, Phys. Rev. Lett. 60 (1980) 1406.
[25] E.Y. Lee, L.J. Schowalter, J. Appl. Phys. 70 (1991) 2156.
[26] A. Blauarmel, M. Brauer, V. Hoffmann, M. Schmidt, Appl. Surf. Sci. 166 (2000) 108.
[27] H. Palm, M. Arbes, M. Schulz, Phys. Rev. Lett. 71 (1993) 2224.
[28] C. Manke, Y. Bodschwinna, M. Schulz, Appl. Sur. Sci. 117/118 (1997) 321.
[29] T. Sumiya, T. Miura, H. Fujinuma, S. Tanaka, Appl. Surf. Sci. 117/118 (1997) 329.
[30] T. Kılıçoğlu, S. Asubay, Physica B 368 (2005) 58.
[31] E.H. Nicollian, A. Goetzberger, Appl. Phys. Lett. 7 (1965) 216.
[32] A. Singh, Solid State Electron 28 (3) (1985) 223.
[33] A. Türüt, B. Bati, A. Kökçe, M. Sağlam, N. Yalçın, Phys. Scr. 53 (1996) 118.
[34] A. Türüt, N. Yalçın, M. Sağlam, Solid State Electron 35 (1992) 835.
[35] M. Sağlam, E. Ayyıldız, A. Gümüş, A. Türüt, H. Efeoğlu, S. Tüzemen, Appl. Phys. A 62 (1996) 269.
[36] A. Singh, J. Appl. Phys. 68 (7) (1990) 3475.