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Frequency and gate voltage effects on the dielectric properties of Au/SiO_2/*n*-Si structures

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ABSTRACT

To determine the dielectric constant (ε'), dielectric loss (ε''), loss tangent ($\tan\delta$), the ac electrical conductivity (σ_{ac}) and the electric modulus of Au/SiO_2/*n*-Si structure, the measurement admittance technique was used. Experimental results show that the values of ε', ε'', $\tan\delta$, σ_{ac} and the electric modulus show fairly large frequency and gate bias dispersion especially at low frequencies due to the interface charges and polarization. An increase in the values of the ε' and ε'' were observed with both a decrease in frequency and an increase in frequency. The σ_{ac} is found to increase with both increasing frequency and voltage. In addition, the experimental dielectrical data have been analyzed considering electric modulus formalism. It can be concluded that the interface charges and interfacial polarization have strong influence on the dielectric properties of metal–insulator–semiconductor (MIS) structures especially at low frequencies and both in depletion and accumulation regions.

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1. Introduction

The metal–insulator–semiconductor (MIS) structures or metal–oxide–semiconductor (MOS) consist of an insulator layer between metal and semiconductor. This insulator layer cannot only prevent inter-diffusion between metal and semiconductor substrate, but also alleviate the electric field reduction issue in these structures. An insulator layer in these structures gives these devices the properties of a capacitor, which stores the electric charge, by virtue of the dielectric properties of oxide layers. The presence of interfacial insulator layer and interface states at M/S interface strongly influences both the electrical and dielectric behavior of these structures. The formation of an insulator layer on Si by traditional ways of oxidation or deposition cannot completely passivate the active dangling bonds at the semiconductor surface. At high angular frequencies ($\omega = 2\pi f$), the carrier life time τ is much larger than the period ($T = 1/\omega$), the charges at the interface states cannot follow an ac signal. In contrary, at low frequencies the charges can easily follow an ac signal and so the effect of these charges on the capacitance of devices increases with decreasing frequency. Therefore, the frequency dependent electrical and dielectric characteristics are very important according to accuracy and reliability result [1–13]. When localized interface states exist at the Si/SiO_2 interface and the device behavior is different from the ideal case due to their presence. These interface states usually cause a bias shift and frequency dispersion of the *C–V* and *G–V* curves [14]. Therefore, it is important to include the effect of the frequency and examine in detail the frequency dispersion of dielectric properties. The frequency response of the dielectric constant (ε'), dielectric loss (ε'') and dielectric tangent ($\tan\delta$) is dominated by a low frequency dispersion, whose physical origin has long been in question [7].

In our previous work [15], we investigated the frequency dependence of the forward and reverse bias *C–V* and *G/w–V* characteristics of Au/SiO_2/*n*-Si structures at room temperature. The aim of this study is to investigate the effect of the frequencies and gate bias on dielectric properties of MIS structures by using the forward and reverse bias admittance measurements over the frequency and gate bias range of 1 kHz–1 MHz and −8 V to 8 V, respectively. Experimental results show that the dielectric properties have been found a strong function of frequencies and bias voltage.

2. Experimental procedure

The metal–insulator–semiconductor (Au/SiO_2/*n*-Si) structures used in this study were fabricated using *n*-type (Phosphor-doped) single crystal silicon wafer with <1 0 0> surface orientation, having thickness of 280 μm, 2″ diameter and 8 Ω cm resistivity. For the fabrication process, Si wafer was degreased in organic solvent of CHClCCl2, CH3COCH3 and CH3OH, etched in a sequence of H2SO4 and H2O2, 20% HF, a solution of 6HNO3:1HF:35H2O, 20% HF and finally quenched in de-ionized water of resistivity of

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18 MΩ cm for a prolonged time. High purity (99.999%) gold (Au) with a thickness of ∼2000 Å was thermally evaporated from the tungsten filament onto the whole backside of in half wafer at a pressure of $\sim 2 \times 10^{-6}$ Torr in vacuum evaporation system. The ohmic contacts were prepared by sintering the evaporated Au back contact at 650 °C for 45 min in flowing dry nitrogen ambient at rate of 2 l/min. This process served both to sinter the Au and to form the required insulator layer (SiO_2) on the upper surface of the Si wafer. After the thermal treatment the wafer was placed in the vacuum system and Au rectifier contacts (dots) with thickness of 2000 Å were deposited at a rate of 4 Å/s through a metal shadow masks with circular dots of ∼2.5 mm diameter. The metal thickness layer

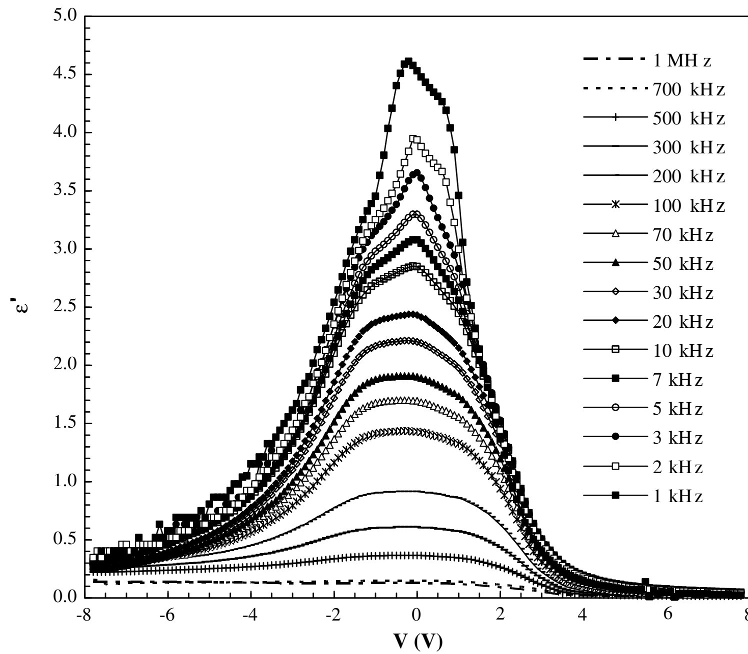

Fig. 1. The variations of the dielectric constant vs. applied voltage for various frequencies of $Au/SiO_2/n$-Si (MIS) structure at room temperature.

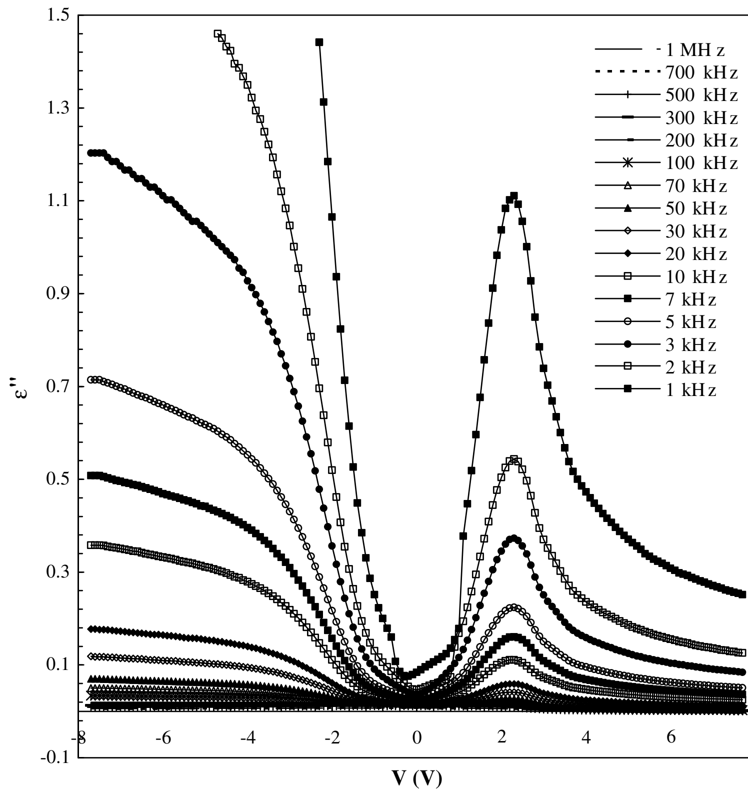

Fig. 2. The variations of dielectric loss vs applied voltage for various frequencies of $Au/SiO_2/n$-Si (MIS) structure at room temperature.

and the deposition rates were monitored with the help of quartz crystal thickness monitor. In this way, metal–semiconductor (MS) structure with thin interfacial insulator layer (SiO_2) was fabricated on *n*-type Si. The interfacial layer thickness was estimated to be about 25 Å from high frequency (1 MHz) measurement of the oxide capacitance in the strong accumulation.

The frequency dependent of the reverse and forward bias capacitance–voltage (*C–V*) and conductance–voltage (*G*/ω–*V*) measurements of MIS structures are carried out in the frequency range of 1 kHz–1 MHz by using a HP 4192A LF impedance analyzer (5 Hz–13 MHz) and a small sinusoidal signal of 40 mV_{p-p} from the external pulse generator is applied to the sample in order to meet the requirement [1]. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. Results and discussion

The frequency dependence of dielectric constant (ε'), dielectric loss (ε''), loss tangent ($\tan\delta$), ac electrical conductivity (σ_{ac}) and electric modulus were evaluated from the knowledge of capacitance and conductance measurements for Au/SiO_2/*n*-Si (MIS) structure in the frequency range of 1 kHz–1 MHz, at room temperature. The complex permittivity can be written [16,17] as

$$\varepsilon^* = \varepsilon' - i\varepsilon'' \tag{1}$$

where ε' and ε'' are the real and the imaginary of complex permittivity, and i is the imaginary root of -1. The complex permittivity formalism has been employed to describe the electrical and dielectric properties. In the ε^* formalism, in the case of admittance Y^* measurements, the following relation holds

$$\varepsilon^* = \frac{Y^*}{j\omega C_o} = \frac{C}{C_o} - i\frac{G}{\omega C_{o_i}} \tag{2}$$

where, C and *G* are the measured capacitance and conductance of the dielectric material (SiO_2) and ω the angular frequency ($\omega = 2\pi f$) of the applied electric field [18].

The real part of the complex permittivity, the dielectric constant (ε'), at the various frequencies is calculated using the measured capacitance values at the strong accumulation region from the relation [19,20],

$$\varepsilon' = \frac{C}{C_o} - \frac{Cd_i}{\varepsilon_o A} \tag{3}$$

where C_o is capacitance of an empty capacitor, *A* is the rectifier contact area of MIS structure in cm^{-2}, d_i is the interfacial insulator layer thickness and ε_o is the permittivity of free space charge ($\varepsilon_o = 8.85 \times 10^{-14}$ F/cm). In the strong accumulation region, the maximal capacitance of MIS structure corresponds to the insulator capacitance (C_i) ($C_{ac} = C_i = \varepsilon'\varepsilon_o A/d_i$). The imaginary part of the complex permittivity, the dielectric loss (ε''), at the various frequencies is calculated using the measured conductance values from the relation,

$$\varepsilon'' = \frac{G}{\omega C_i} = \frac{Gd_i}{\varepsilon_o \omega A} \tag{4}$$

The loss tangent ($\tan\delta$) can be expressed as follows [11,16,17,19,20],

$$\tan\delta = \frac{\varepsilon'}{\varepsilon''} \tag{5}$$

The ac electrical conductivity (σ_{ac}) of the dielectric material can be given by the following equation [16,21,22],

$$\sigma_{ac} = \omega C \tan\delta(d/A) = \varepsilon''\omega\varepsilon_o \tag{6}$$

The complex impedance (Z^*) and complex electric modulus (M^*) formalisms were discussed by various authors with regard to the analysis of dielectric materials [18,22]. Analysis of the complex permittivity (ε^*) data within the Z^* formalism ($Z^* = 1/Y^* = 1/i\omega C_o\varepsilon^*$) is commonly used to separate the bulk and the surface phenomena and to determine the bulk dc conductivity of the material [11,21]. The complex impedance or the complex permittivity ($\varepsilon^* = 1/M^*$)

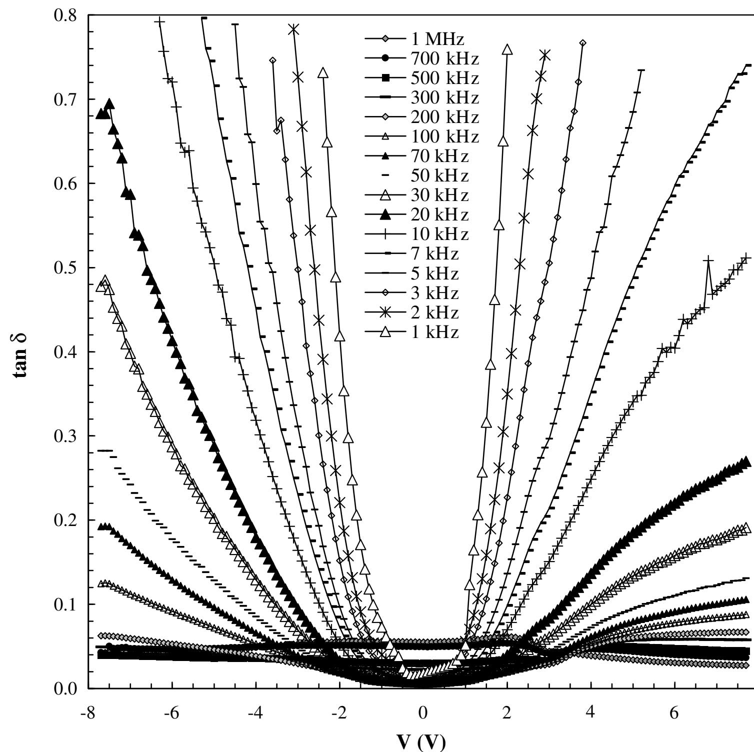

Fig. 3. The variations of tangent loss vs applied voltage for various frequencies of Au/SiO_2/*n*-Si (MIS) structure at room temperature.

data were transformed into the M^* formalism using the following relation [18,22,23]

$$M^* = i\omega C_o Z^* \tag{7}$$

or

$$M^* = \frac{1}{\varepsilon^*} = M' + jM'' == \frac{\varepsilon'}{\varepsilon'^2 + \varepsilon''^2} + j\frac{\varepsilon''}{\varepsilon'^2 + \varepsilon''^2} \tag{8}$$

The real component M' and the imaginary component M'' were calculated from ε' and ε''.

Figs. 1–3 show the ε'–V, ε''–V and $\tan\delta$–V curves for Au/SiO_2/n-Si (MIS) structure at various frequencies, respectively. As can be seen in these figures, the values of ε', ε'' and $\tan\delta$ are strongly dependent on both frequency and applied bias voltage. As shown from Figs. 1 and 2, both the ε'–V and ε''–V characteristics have an anomalous peak. The peak values ε'–V and ε''–V have decreased with increasing frequency and the peak positions slightly shift towards inversion region.

The peak value of the ε' and ε'' stem from measurements capacitance and conductance values, respectively and such behaviors depend on a number of parameters such as doping concentration, interface state density, series resistance of diode and the thickness of the interfacial insulator layer[24]. It is well known that the capacitance and conductance are extremely sensitive to the interface properties and series resistance [1,25–27]. This occurs because of the interface states that respond differently to low and high frequencies. Similar results have been reported in the literature [28] and they ascribed such a peak to only interface states.

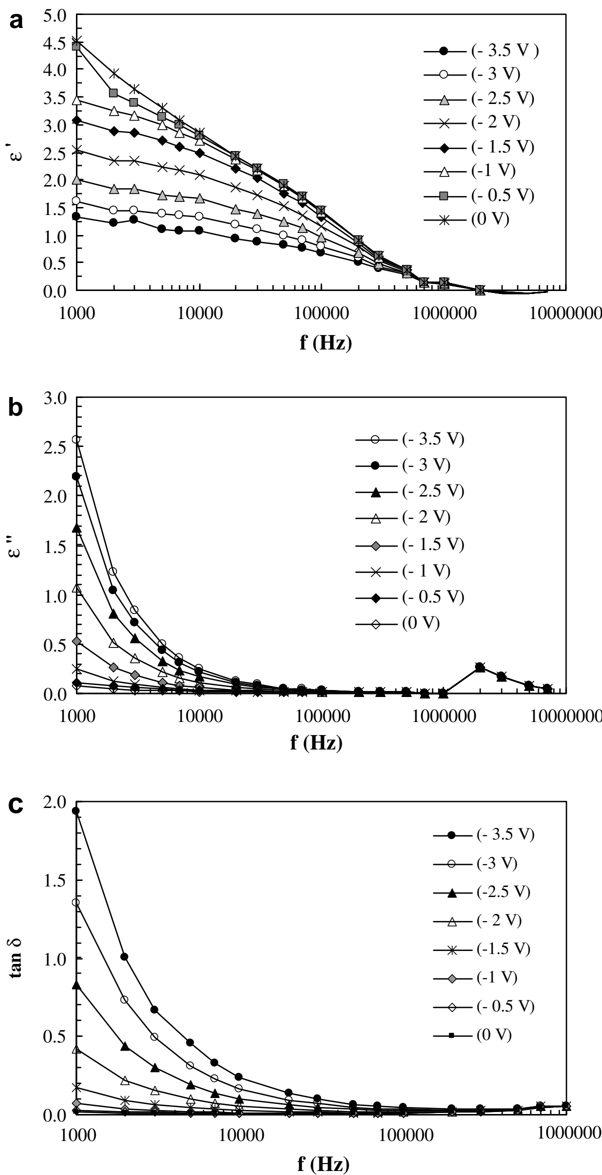

Fig. 4. Frequency dependence of the (a) ε', (b) ε'' and (c) $\tan\delta$ for various applied voltage of Au/SiO_2/n-Si (MIS) structure at room temperature.

The frequency dependencies of the ε', ε'' and $\tan\delta$ of Au/SiO_2/n-Si (MIS) structure at different voltage are presented in Fig. 4a, b and c, respectively. The values of the ε', ε'' and $\tan\delta$ obtained from the measured capacitance and conductance were found a strong function of applied voltage especially at low frequencies. As can be seen from these figures, ε' and ε'' decrease as the frequency are increased. Also, it is clearly seen in Fig. 4, that the values of ε', ε'' and $\tan\delta$ of Au/SiO_2/n-Si (MIS) structure are almost independent of voltage at high frequencies. In principle, at low frequencies, all the four types of polarization processes, i.e., the electronic, ionic, dipolar, and interfacial or surface polarization contribute to the values of ε' and ε''.

On raising frequency, the contributions of the interfacial, dipolar or the ionic polarization become ineffective leaving behind only the electronic part. Furthermore, the decrease in ε' and ε'' with increase in frequency is explained by the fact that as the frequency is raised, the interfacial dipoles have less time to orient themselves in the direction of the alternating field [29–35]. Especially, in the high frequency range, the values of ε' become closer to the values of ε''. This behavior of ε' and ε'' may be due to the interface states can not follow the ac signal at high frequency. The carrier lifetime of interface trapped charges (τ) are much larger than $1/\varepsilon$ at very high frequency (ω), i.e., the charges at interface cannot follow an ac signal. Such as behavior was observed by several authors [27,31,36–39].

The variation of the loss tangent ($\tan\delta$) with respect to frequency of MIS structure at different voltages is shown in Fig. 4c. As shown in Fig. 4c, the $\tan\delta$ decreases with increasing frequency but remain constant at high frequencies. This behavior is like behaviors of ε' and ε''.

The ac electrical conductivity (σ_{ac}) of the MIS structure at different voltage is presented in Fig. 5. It is noticed that the dc conductivity is generally increased with increasing the frequency and especially there is a sharp increase in the σ_{ac} after about

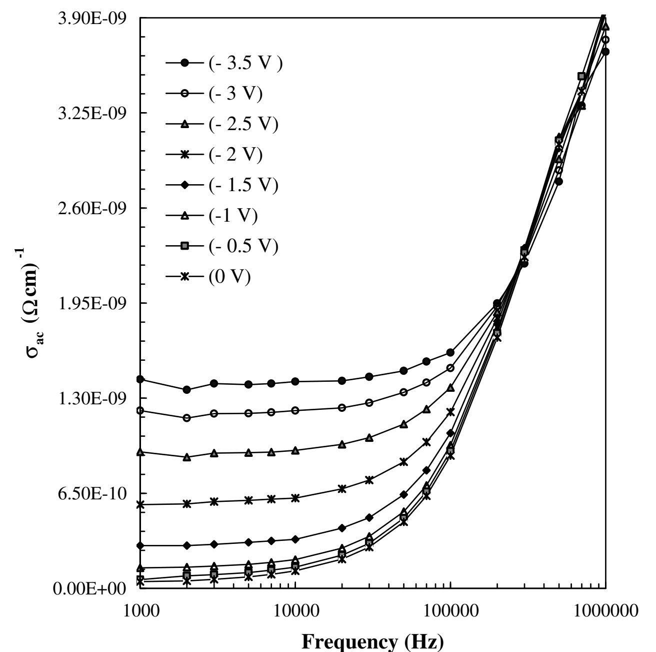

Fig. 5. Frequency dependence of ac electrical conductivity (σ_{ac}) for various applied voltage of Au/SiO_2/n-Si (MIS) structure at room temperature.

100 kHz. At the same time the values of σ_{ac} are almost independent of voltage at high frequencies. This dc conductivity contributes only to the dielectric loss, which becomes infinite at zero frequency and important at high frequencies [40]. Similar behavior was observed in the literature [23,29–31,35,41,42].

The complex modulus analysis is based on the plot of the real part of M' against the imaginary part of M'' over a wide range of frequencies, 1 kHz–1 MHz in the present study.

Fig. 6a and b have shown the M' and M'' of electric modulus M^* versus frequency for MIS structure at room temperature. As can be seen from Fig. 6a and b, M' and M'' increase as the frequency are increased and especially there is a sharp increase in the M' and M'' in the frequency range between 500 kHz and 1 MHz. Similar studies have been reported in literature [18,22,23,29].

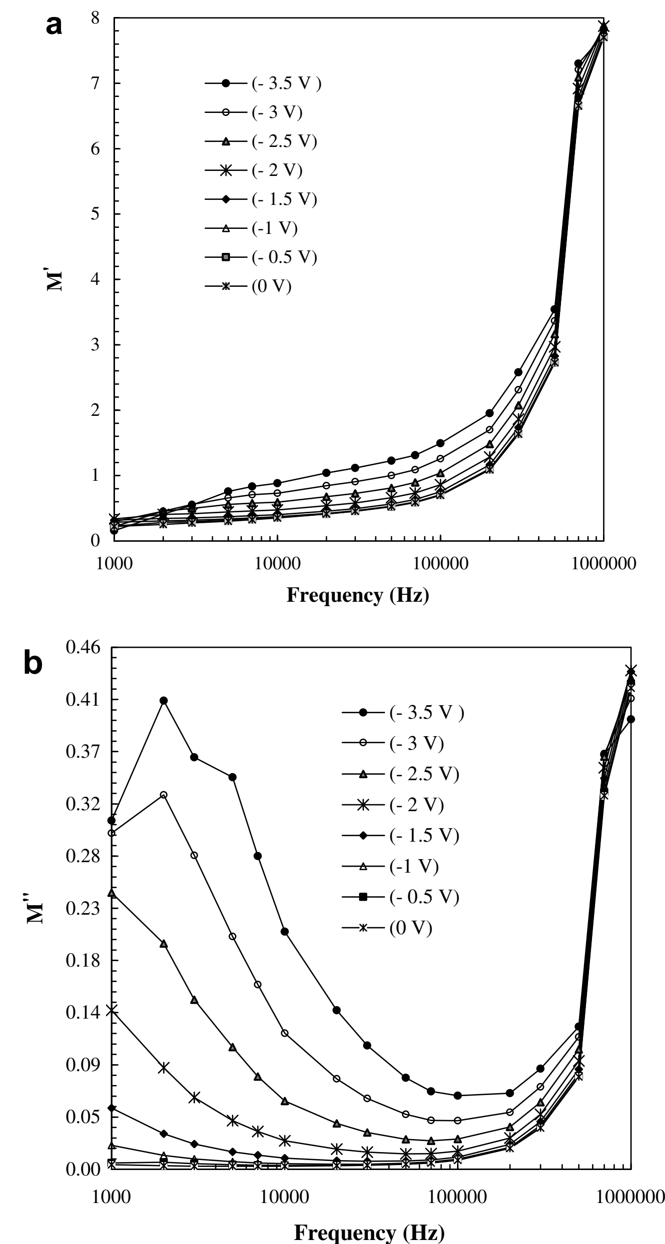

Fig. 6. (a) The real part M' and (b) the imaginary part M'' of electric modulus M^* vs frequency for MIS structure at room temperature.

4. Conclusions

The frequency dependence of dielectric properties of Au/SiO_2/n-Si (MIS) structures has been studied in detail in the wide frequency range of 1 kHz-1 MHz at room temperature. Experimental results show that the values of ε', ε'', $\tan\delta$, σ_{ac} and the electric modulus show fairly large frequency and gate bias dispersion especially at low frequencies. This behavior is attributed to the interface charges and polarization. Also interface states can easily follow the ac signal at low frequencies and yield an excess capacitance and conductance, which depends on the relaxation time of the interface states and the frequency of ac signal. The ac electrical conductivity (σ_{ac}) increases with increasing frequency. In addition, the experimental dielectrical data have been analyzed considering electric modulus formalism. The behavior of dielectric properties especially depends on frequency, interfacial insulator layer and the density of interface states. Due to the presence of the interfacial insulator layer, interface states and fixed surface charges cause the deviation from the ideal behavior of the dielectric characteristics.

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