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Characterization of GZO thin films fabricated by RF magnetron sputtering method and electrical properties of In/GZO/Si/Al diode

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Abstract
The main focus of this work is the structural and optical characterization of Ga-doped ZnO (GZO) thin film and determination of the device behavior of In/GZO/Si/Al diode. GZO thin films were deposited by RF magnetron sputtering technique from single target. The structural and morphological properties of GZO film were investigated by X-ray diffraction (XRD), Raman scattering, scanning electron microscopy (SEM) and energy dispersive X-ray spectroscopy analysis (EDS) measurements. Optical properties of the film were determined with transmission measurement. Device characterization of In/GZO/Si/Al diode were done with the analysis of temperature dependent current voltage (*I–V*) measurement. The current conduction mechanism was investigated with the Thermionic Emission (TE) method. The deviation from the pure TE method was observed and this deviation was analyzed under the assumption of Gaussian Distribution (*GD*) of barrier height (*TE* emission with *GD*). The mean standard deviation and zero bias barrier height were calculated as 0.0268 (about %3) and 1.239 eV, respectively. Richardson constant was found to be as 115.42 A/cm^2 K^2 using the modified Richardson plot. In addition, series resistance R_s was obtained using Cheung's function. Finally, the interface state densities D_{it} were determined by using the forward bias *I–V* results.

Keywords Ga-doped ZnO · Thin film · Gaussian distribution · Interface states

1 Introduction

Transparent conducting oxides (TCOs) have been intensively investigated for electrical and optical applications such as solar cells, liquid crystal displays, organic light-emitting diodes, photodetectors and flat panel displays due to their low cost, resource availability, and nontoxicity [1–3]. Mostly, indium tin oxide (ITO) is used for the optoelectronic applications due its high transmittance and low resistivity [4]. On the other hand, ITO has some drawbacks such as low stability, high cost having rare material and having toxicity due containing indium. Hence, developing an alternative TCO for ITO or limiting the indium usage in TCOs is an important problem [5]. Doped ZnO materials have been promising candidate as non-toxic and cheap alternative to ITO [6].

The electrical and optical characteristics of ZnO could be improved with substitution of Zn^{2+} cations with group III elements. Various dopants could be used such as Al, Co and In [6–8]. Among these dopants, Ga cation is currently regarded as a better substitutional dopant and Ga-doped ZnO (GZO) has been promising candidate for ITO due having low cost and excellent optical and electrical properties [9].

GZO thin films have been fabricated by using various techniques such as chemical vapor deposition, sol-gel method, pulsed laser deposition (PLD) [10–12]. Among these techniques, magnetron sputtering has been one of the favored due having outstanding properties such as its simplicity, high deposition velocity and low operating temperature. Moreover, single crystal thin films with high-quality are fabricated by using magnetron sputtering combined with RF power. Besides, the option of low substrate temperature during the fabrication process enable the use of large variety substrates such as flexible ones [7, 13].

In the present work, %1.5 Ga doped ZnO (GZO) thin films, were fabricated onto Si and glass substrates by RF

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magnetron sputtering method at room temperature, were studied in terms of material with the opportune on deposition from single GZO target at room temperature. Structural properties of GZO thin film deposited onto glass substrate was investigated in terms of X-ray diffraction (XRD), Raman measurement, scanning electron microscope (SEM) imaging and energy dispersive X-ray spectroscopy (EDS) analysis. And, optical properties of GZO thin film was determined by using transmission measurements.

In addition, there are very limited study for the electrical properties of ZnO/Si diodes analyzed with using temperature dependent *I–V* characteristics and modeled by TE model with modified by Gaussian distribution of the barrier height [14]. On the contrary, there are the lack of studies about current conduction mechanism and interface properties for GZO/Si diodes. In the present study temperature dependent, *I–V c*haracteristics was also modeled by TE model with modified by Gaussian distribution of the barrier height for In/GZO/Si/Al diode and interface state densities in this diode was determined.

2 Experimental details

GZO thin films were deposited by RF magnetron using single Ga doped ZnO sputtering target (containing 3 wt% Ga_2O_3). The substrate temperature was kept around room temperature. The base vacuum of the deposition system was around 10^{-6} Torr. And, during the deposition, with the pure argon flow to the chamber it was reached at 10^{-3} Torr.

In order to determine the physical and optical properties of GZO thin film, soda lime glass (SLG) substrate was used and the same procedures was applied as in the previous study for substrates cleaning [15]. The crystal properties of GZO film deposited onto SLG were analyzed by X-ray diffraction (XRD) system, which is Rigaku Miniflex model, equipped with the radiation source having the source wavelength of $\lambda = 1.54$ Å (Cu-Kα). Raman analysis was carried out at room temperature using a Horiba-Jobin Yvon i550 system equipped with a CCD camera with 1 cm^{-1} resolution and a laser with the wavelength of 532 nm used as an excitation source. Scanning electron microscope (SEM) which is Zeiss EVO15 model was used to obtain the surface image. And, Energy dispersive X-ray spectroscopy (EDS) detector which is attached to SEM was used to determine the composition of GZO film. Additionally, Optical transmission measurement was done with using PerkinElmer Lambda 45 UV/VIS/NIR spectrophotometer in the wavelength range of 300–1100 nm.

The In/GZO/Si/Al diode was fabricated by deposition of GZO thin film layer on p-type Si wafer having (111) crystal orientation and the resistivity value of 1–10 (Ω cm). Before the deposition of GZO layer, the back ohmic contact with Al was formed. After deposition of GZO layer onto Si wafer with back contact, top ohmic contact layer was deposited by thermally evaporated In. The electrical characteristic of In/GZO/Si/Al diode was determined by temperature dependent current–voltage *I–V* measurements under dark condition. Keithley 2401 source-measure unit was used and the sample temperature was scanned from 220 to 360 K by the help of CTI-Cryogenics Model 22 refrigerator system combined with Model SC helium compressor. In this measurement system, the temperature of the sample was controlled and monitored by using Lakeshore DRC-91C controller.

3 Results and discussion

3.1 Material properties of GZO thin film layer

XRD measurement was carried out to determine the structural properties of GZO thin film. Figure 1a illustrates the XRD patterns of GZO thin film deposited onto glass substrate. There is a dominant diffraction peak around angle of 34.6, which corresponds to the crystalline orientations in the plane directions of (002). This result indicates that the film show a preferred orientation with the c-axis perpendicular to the substrate [16–19].

The structural quality of GZO thin film was identified by calculating the structural parameters. The average grain size was calculated by using Scherrer formula and it was found to be as 7.71 nm [20]. Moreover, parameters for dislocation density (δ), microstrain (ε) and lattice strain,which are related to the crystal defect and lattice mismatch in the structure, were calculated as 1.68×10^{11} m, 0.005 and 0.016, respectively [20, 21].

Raman measurement was also carried out to verify the phase purity of GZO structure, using 532 nm laser excitation source. Figure 1b shows the Raman shifts of GZO thin film centered at 280 and 580 cm^{-1}. When compared to the observed results with the literature, the peak around 280 cm^{-1} belongs to A_1(TO) mode and the peak around 582 cm^{-1} belongs to E_1(LO) mode for the structure of 1–5% Ga-doped ZnO [22].

EDS and SEM measurements were done for the compositional analysis and surface properties of the GZO thin film. EDS result shown in Fig. 2 indicates that the atomic percentage of Ga in the structure is about 1.50%. By considering the Raman shifts which belongs to the doping percentage in the range of 1to 5 %, the Ga doping percentage obtained from EDS anlysis is in a consistent with the literature [22]. In addition, SEM image given in Fig. 2 shows that GZO thin film has almost a uniform surface.

Transmission measurement at room temperature was carried out in the wavelength range of 300–1100 nm. As seen in Fig. 3, GZO thin film has very high tranparency and in the visible region it has the maximum value about

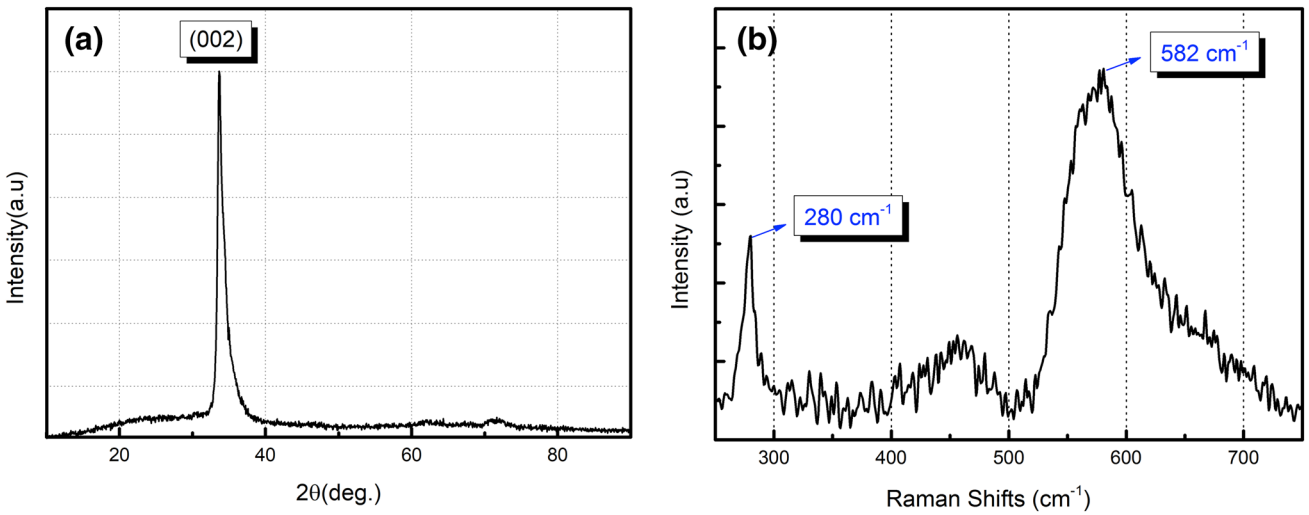

Fig. 1 XRD pattern (**a**) and Raman shifts (**b**) of GZO thin film deposited onto glass substrate

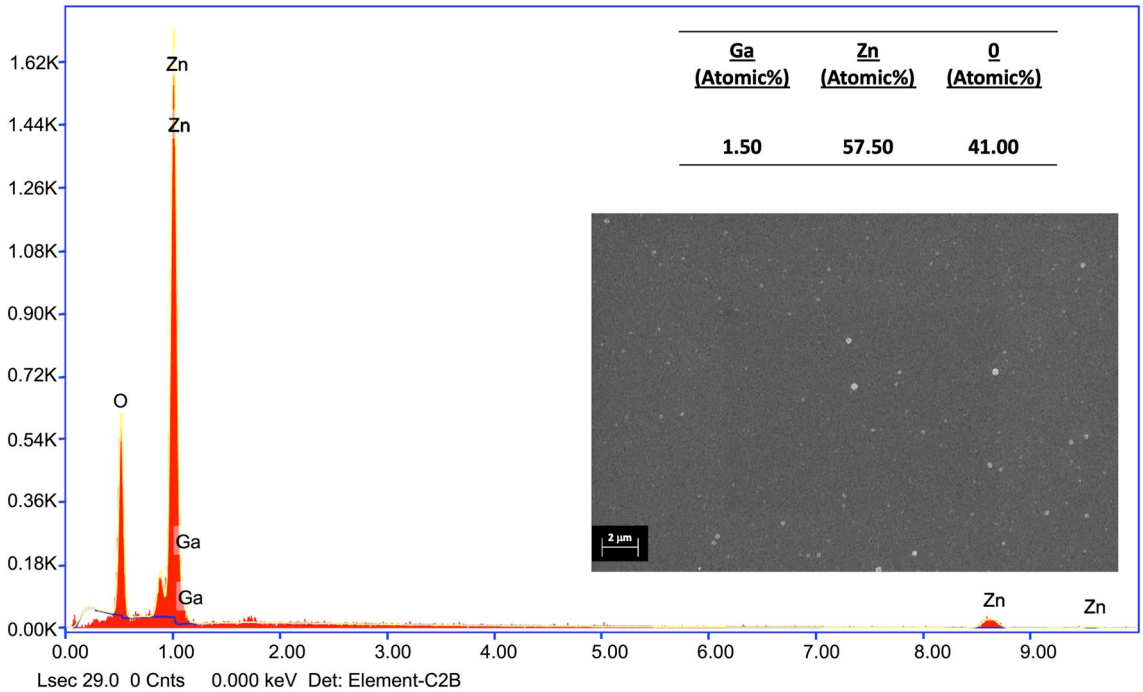

Fig. 2 EDS result and SEM image of GZO thin film

98%. The absorption coefficient was calculated from the transmission spectra by using Tauc plot as inserted in Fig. 3 [23]. The direct band gap energy of GZO thin films was found to around 3.23 eV. The band gap value of ZnO structure increases from 3.18 to 3.25 eV as the Ga dopant values increased from 0 to 5 at.% [24]. Hence, the obtained result for deposited GZO thin film is in a good agreement with the literature.

3.2 Device properties of In/GZO/Si/Al diode

The schematic illustration and the energy-band diagram of the fabricated In/GZO/Si/Al diode are shown as inset in Fig. 4a and b, respectively. This diode was characterized under the results of temperature dependent *I–V* measurements. According to this analysis, diode parameters were calculated as a function of sample temperature and possible conduction

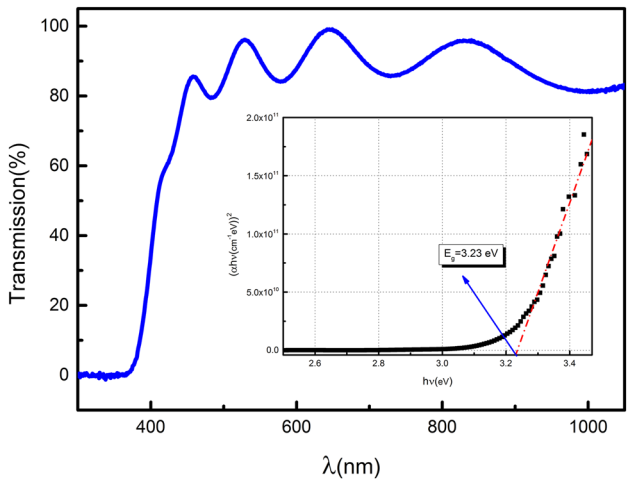

Fig. 3 Transmission spectrum in the wavelength range of 300–1100 nm and corresponding Tauc plot (inset) of GZO thin film

mechanisms were analyzed. In addition, Room Temperature *I–V* measurement for In/GZO (see Fig. 4right hand side) was carried out to indicate the electrical behavior of In/GZO layers. As seen from the figure, In/GZO layer shows ohmic behavior.

The *I–V* characteristics of In/GZO/Si/Al diode have a rectifying nature with a rectification factor above two orders of magnitude for each temperature region. The current transport through this diode structure was discussed by considering thermionic emission (*TE*) model. At the forward bias region, the current through the junction is given with the deviation from ideality as [25–27];

$$I = I_0\left[exp\left(\frac{q(V - IR_s}{nkT}\right) - 1\right] \tag{1}$$

where the assumption of $V > 3kT/q$ with excluding possible effects of reverse current contribution is valid and I_0 is the saturation current, q is the electron charge, IR_S term is the voltage drop under the effect of series resistance R_s, n is the ideality factor depending on the current transport mechanism through the junction, k is the Boltzmann constant and T is the temperature of interest [28, 29]. By using the obtained *I-V* data given in Fig. 4, I_0 values were obtained from of the straight-line region of *I–V* plot at zero bias and they were tabulated in Table 1. In addition, it is given as [30, 31];

$$I_0 = AA^* exp\left(-\frac{q\phi_{b0}}{kT}\right) \tag{2}$$

where A represents the effective diode area and A^* is Richardson constant. $\phi_{b0}$is the zero bias barrier height and it could be calculated for each temperature from the values of I_0 as;

$$\phi_{bo} = \frac{kT}{q}\, ln\left(\frac{AA^*T^2}{I_o}\right) \tag{3}$$

The temperature dependence of calculated ϕ_{b0} values is shown in Fig. 5a. As seen in the figure, there is an increasing trend for ϕ_{b0} values with increasing temperature. The behavior in ϕ_{b0} with the change in T showed that current transport across the interface is temperature excited process. For the *TE* approximation case, when the temperature increases, the number of carriers start to have sufficient thermal energy. Hence, they can overcome the high barriers [15, 16].

Moreover, the quality and the determination of the dominant conduction mechanism of the fabricated junction can be identified with the diode ideality factor (n). With the contribution of Eq.1, the n values could be obtained by the given equation as below;

$$n = \frac{q}{kT}\left(\frac{dV}{dLn(I)}\right) \tag{4}$$

n values were determined for each temperature and the obtained values given in Table 1. Also, the temperature dependence of these values is shown in Fig. 5a. Figure 5a indicates that there is a decreasing trend with increasing temperature for the n values while an opposite situation is valid for ϕ_{b0} values.

The contrast of the temperature dependence in betweenϕ_{b0} and n values might be due to the formation of inhomogeneous barrier height formation by the presence of the interfacial layer and also non-uniformity of the interfacial charges and recombination current through the interfacial states of the junction [32–34]. Moreover, the higher than unity value of n can be the indication of laterally inhomogeneity in diode structures [35]. Hence, these situations resulted in the deviation from the pure *TE* model and the additional current transport mechanism to *TE* model should be required to determine the conduction in the junction. Figure 5b illustrates the relation in between ϕ_{b0} and n values. As seen from the figure, an inverse proportion is the indication of the lateral inhomogeneity in the barrier height [36, 37]. A lateral barrier height which is also known as a laterally homogeneous value of barrier height was found to be as about 1.23 eV under the consideration of Tung's approach from the extrapolation of Fig. 5b (the ϕ_{b0} value when n =1). This approach indicates that the existence of local non-uniform patches of relatively lower or higher barriers with respect to an average barrier height [38]. The observation of the deviation from an ideal *I–V* characteristics due to the *TE* model in the fabricated structure could be modelled as Gaussian distribution (*GD*) of the barrier height at the junction interface (*TE emission with GD*) [39]. According to *TE* with *GD* model, the current transport mechanism is described in terms of a Gaussian-type function by expanding the barrier height with covering the effect of inhomogeneous barrier formation and the distribution of the

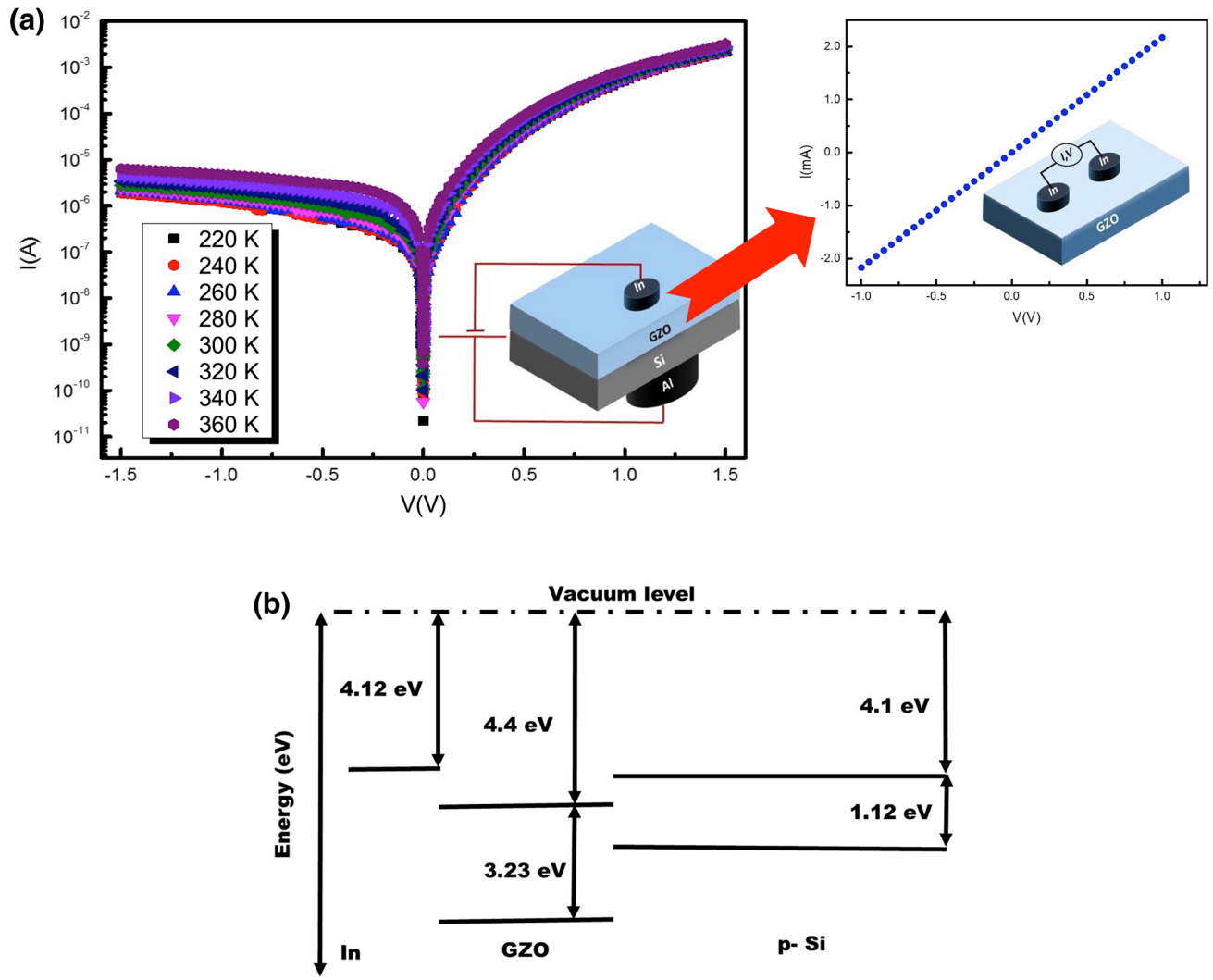

Fig. 4 **a** Temperature dependent I–V characteristics of In/GZO/p-Si/Al (the schematic diagram given as inset) diode and the right hand side of the figure shows the I–V characteristic of In/GZO (the schematic diagram given as inset) at room temperature. **b** The energy band diagram of In/GZO/Si/Al diode

Table 1 The electrical parameters of In/GZO/p-Si/Al diode obtained from temperature dependent *I–V* characteristics

T(K)	Ideality factor (n)	Saturation current (I_0(A) × 10^{-8})	Zero bias barrier height [ϕ_{b0} (eV)]
220	3.13	4.69	0.54
240	2.79	5.49	0.59
260	2.63	5.52	0.64
280	2.54	6.03	0.69
300	2.39	11.40	0.72
320	2.34	16.60	0.76
340	2.33	70.60	0.77
360	2.23	134.00	0.80

inhomogeneity in the barrier. *TE* with *GD* model assumes the total current through the junction as being a sum of the current flows in all individual patches having different lower barrier heights. Hence, the total current through the junction is expressed as;

$$I = AA^{*}T^{2}exp\left[\left(-\frac{qV}{kT}\right)\left(\phi_{b0}-\frac{q\sigma_0^2}{2kT}\right)\right] \times exp\left(\frac{qV}{n_{ap}kT}\right)\left[1-exp\left(-\frac{qV}{kT}\right)\right] \quad (5)$$

And the modified reverse saturation current is given as;

$$I_0 = AA^{*}exp\left(-\frac{q\phi_{ap}}{kT}\right) \quad (6)$$

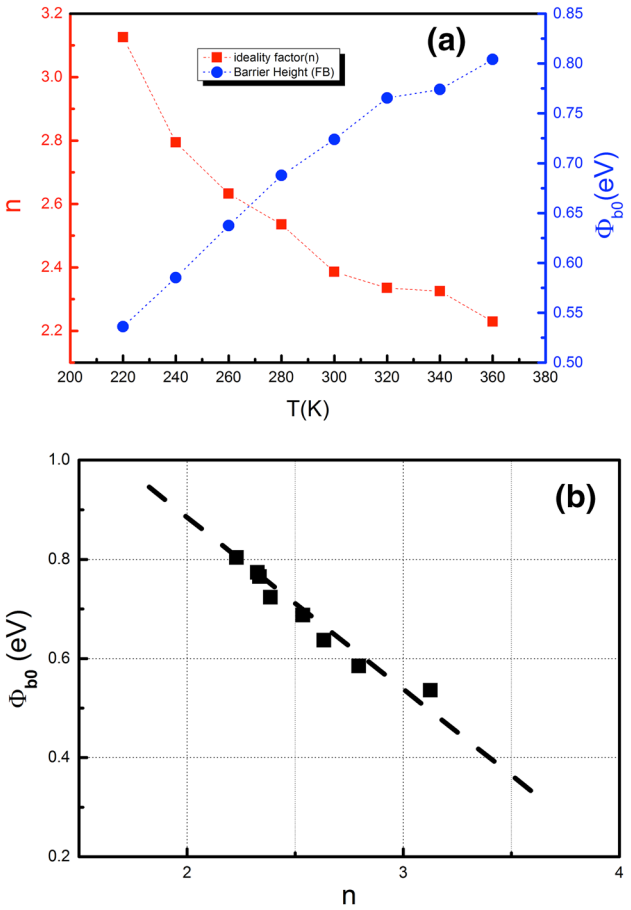

Fig. 5 Variation of $\phi_{b0}$and n with temperature (**a**) and relation between ϕ_{b0} and n (**b**) for In/GZO/p-Si/Al diode

where n_{ap} and ϕ_{ap} represent the apparent ideality factor and apparent barrier height, respectively. By using the *TE* with *GD* model, the temperature dependence of ϕ_{b0} is expressed [40, 41];

$$\phi_{ap} = \bar{\phi}_{b0} - \frac{q\sigma_s{}^2}{2kT} \tag{7}$$

where $\sigma_s$is the standard deviation of barrier height in the temperature variation and it determines the deviation from the homogeneity of barrier height [37, 39]. In addition, $\bar{\phi}_{b0}$is the mean value. With the plot of ϕ_{b0} vs $q/2kT$ (see Fig. 6), σ_s and $\bar{\phi}_{b0}$ values were obtained as 0.0268 (about %3) and 1.239 eV, respectively.

According to *TE* with *GD* model, the modified ideality factors with varying T (n_{ap})were also obtained by using Equation 7 as [39];

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{8}$$

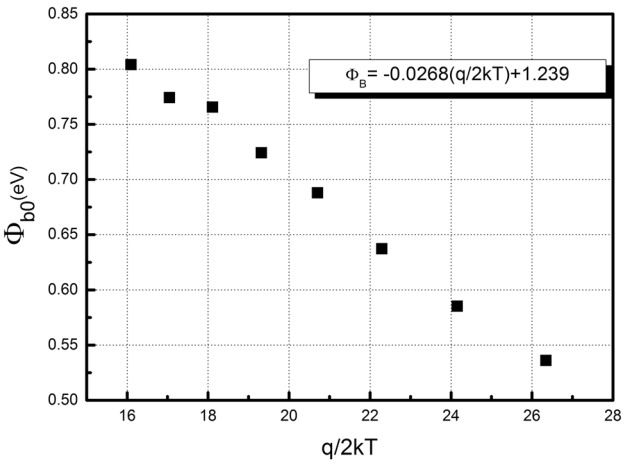

Fig. 6 Plot of ϕ_{b0} vs. $q/2kT$ for for In/GZO/p-Si/Al diode

where the parameters labeled as ρ_2 and ρ_3 are the bias dependence of $\bar{\phi}_{b0}$ andσ_s, respectively. These parameters are related to the voltage deformation of the barrier height distribution. Hence, it could be concluded that Equation (7) expresses the temperature effects on n the ideality factor and it could be a measurement tool to indicate the homogenization of the barrier distribution [39, 42]. By using the plot of (n^{-1}-1) vs. /2kT plot (Fig. 7), ρ_2 and ρ_3 parameters were obtained as 0.03573 and 0.012, respectively.

Moreover, the relation for Richardson constant obtained from pure TE model should be modified with the *GD* approximation [43]. According to the modified *I–V* relationship based on the barrier inhomogeneity, by combining Equations (5) and (6), the relation for Richardson constant could be modified as [42, 44],

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln\left(AA^*\right) - \frac{q\bar{\phi}_{b0}}{kT} \tag{9}$$

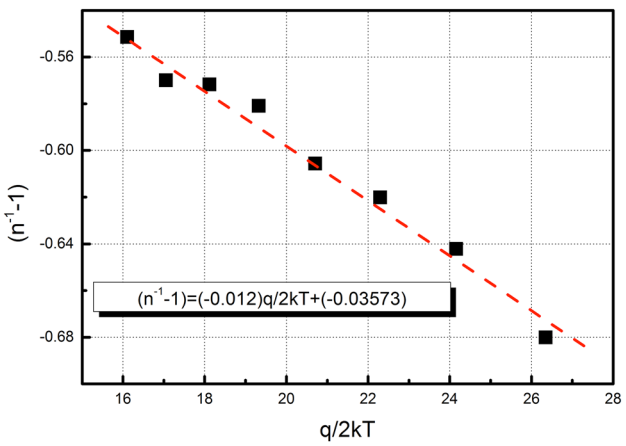

Fig. 7 Plot of $\left(n^{-1} - 1\right)$ vs. $q/2kT$ for for In/GZO/p-Si/Al diode

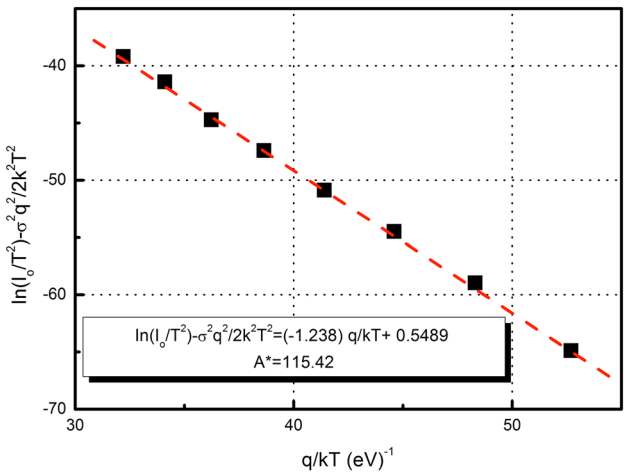

Fig. 8 Plot of $\ln\left(I_0/T^2\right) - \left(q^2\sigma_0^2\right)/\left(2k^2T^2\right)$ vs. q/kT for In/GZO/p-Si/Al diode

The obtained plot of $\ln\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right)$ vs. $\frac{q}{kT}$ is shown in Fig. 8. The slope of this plot gives $\bar{\phi}_{b0}$ and the value of extrapolation determines the modified Richardson constant A^*. The obtained value of $\bar{\phi}_{b0}$ from Fig. 8 is 1.238 eV and this values is consistent with the value obtained from Fig. 6. In addition, the value of A^* was obtained as 115.42 A/cm^{2}K^2 and this value is inconsistent with the expected value of 112 A/cm^{2}K^2 [28].

Mostly, the deviations from the ideal behavior in the forward bias *I–V* measurement (see Fig. 4) could be related to the effect of series resistance R_s. As seen from Fig. 4, at high voltage region of forward bias, the plot is not linear. Hence, R_s is the main responsible of this deviation from the linearity. R_s values were calculated with the method of Cheung and Cheung [45]. In the region where the *I–V* characteristic is not linear in the forward bias, Cheung's function is given as;

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{10}$$

and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*}\right) = n\Phi_b + IR_s \tag{11}$$

Figure 9a shows the *dV/dln(I)* vs. *I* plot and Fig. 9b shows *H(I)* vs. *I* plot for In/GZO/p-Si/Al diode. By considering Cheng's function, Eq. (9) agives a straight line in the region of downward curvature belongs to the forward bias *I–V* characteristics [46]. Hence, the slope of the plot in Fig. 9 will give R_s and the y-axis intercept will give nkT/q. The obtained R_s values as a function of temperature are shown in Fig. 9b. It was concluded that there is a decreasing trend for the Rs values while temperature is increasing. This behavior

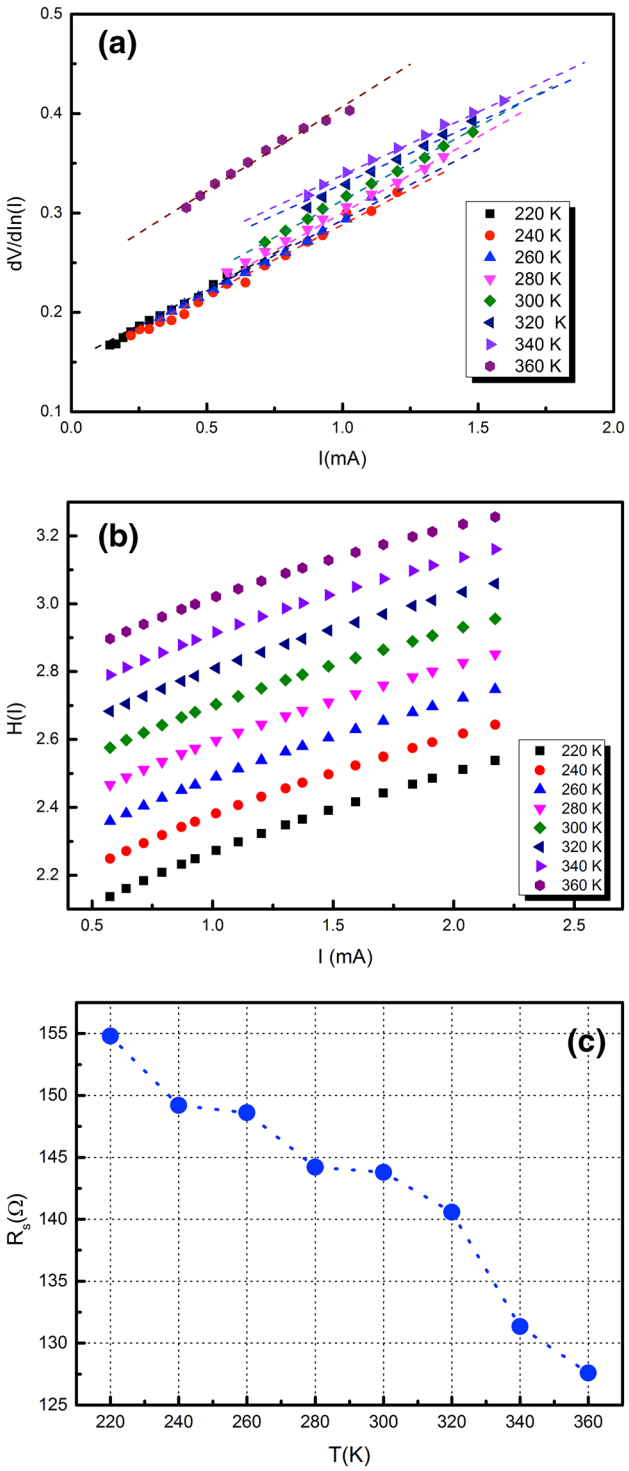

Fig. 9 *dV/dln(I)* vs. *I* plot at different temperatures (**a**), *H(I)* vs. I plot (**b**) and *Rs* vs. *T* (**c**) plot for In/GZO/p-Si/Al diode

is the indication of the lack of free carrier concentration at low temperatures [47, 48].

In addition, the interface state density (D_{it}), affects the device performance, could be determined with the

analysis forward bias *I–V* characteristics by considering the equilibrium of them with the semiconductor [48, 49].

$$D_{it} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n(V) - 1) - \frac{\varepsilon_s}{w_D}\right] \quad (12)$$

Here δ represents thickness of the interfacial insulator layer which was obtained from Eq. (11) by using Capacitance–Voltage (C–V) characteristics at high frequency (not given here) as 6 nanometer. In addition, W_D, which represents the space charge region width, was also obtained from C^{-2} vs. V graph (not given here) [50]. ε_i and ε_s are the permittivity of interfacial insulator layer and semiconductor layer, respectively [51]. And, the n(V) is the voltage dependent ideality factor which was calculated from the Eq. (12);

$$\frac{C_i}{A} = \frac{\varepsilon_i \varepsilon_0}{\delta} \quad (13)$$

$$n(V) = \frac{qV}{kTln\left(\frac{I}{I_0}\right)} \quad (14)$$

The interface layer capacitance given as C_i was calculated from the high-frequency *C–V* and conductance-voltage (*G–V*) measurements (not given here) as;

$$C_i = C_{ma}\left[1 + \left(\frac{G_{ma}}{C_{ma}}\right)^2\right] \quad (15)$$

Here, C_{ma} and G_{ma} represents the measured capacitance and conductance values at the frequency of 2 MHz, respectively.

By taking into account the series resistance R_S, the bias-dependent effective barrier height ϕ_e and the energy of the interface states E_{ss} with respect to the valance band edge E_V ($E_{ss} - E_v$) are calculated by using Eqs. (14) and (15) as [40, 51];

$$\phi_e = \phi_b + \left(1 - \frac{1}{n(V)}\right)(V - IR_s) \quad (16)$$

$$E_{ss} - E_v = q(\phi_e - V) \quad (17)$$

Figure 10a illustrates D_{it} versus $E_{ss} - E_v$ plot in the temperature range of 200 and 360 K. In addition, temperature dependence of D_{it} values are shown in Fig. 10b. As seen in Fig. 10b, there is a decreasing trend for D_{it} values once temperature increases. This behavior may be defined as reordering and restructuring of interface layer's with the temperature effects [35].

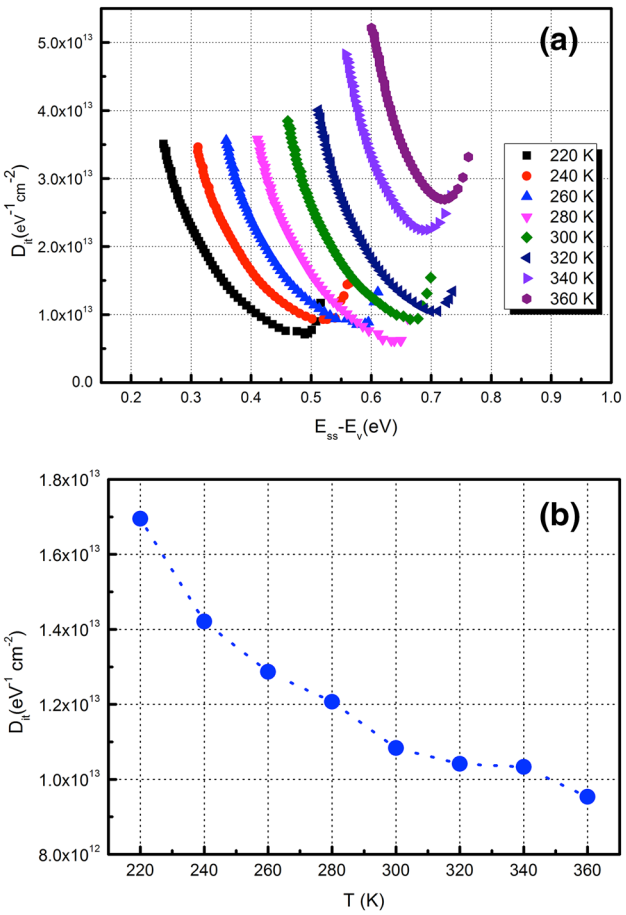

Fig. 10 D_{it} versus $E_{ss} - E_v$ (**a**) and T dependence of D_{it} values (**b**) for In/GZO/p-Si/Al diode

4 Conclusion

In the present study, structural and optical characteristics of GZO thin films deposited onto glass substrate and the device behavior of In/GZO/Si/Al diode were investigated. XRD measurements showed that GZO films have the crystalline orientations in the plane directions of (002).

Raman measurements of GZO thin films indicated that the shift around 280 cm^{-1} belongs to A_1(TO) mode and the shift around 582 cm^{-1} belongs to E_1(LO) mode. EDS analysis revealed that the atomic percentage of Ga in the structure is about 1.50% and this result is inconsistent with both XRD and Raman measurement results. In addition, It was found that, GZO thin films have very high tranparency in the visible region which is about 98% and the band gap energy of GZO thin films is around 3.23 eV. By considering the Ga dopant in the film structure, this values is about the expected value.

The device properties of In/GZO/Si/Al diode was investigated considering *TE* theory by the analysis of temperature dependent forward bias *I–V* in the temperature range of

220–360 K. It was found that n values decreased while ϕ_{b0} values increased with increasing temperature which was the indication of the deviation from pure *TE* theory. The deviation from *TE* theory was estimated with a Gaussian distribution of the barrier height. According to *TE* with *GD* model, the Richardson constant was found to be as 115.42 A/cm^{2}K^2 and this value is inconsistent with the expected value of 112 A/cm^2 K^2. The R_s values were determined using Cheung's function and a decreasing trend for the Rs values while temperature is increasing was observed which is the indication of the lack of free carrier concentration at low temperatures. Moreover, D_{it} values were investigated with the analysis of the f bias I–V results. A decrease tendency with increasing temperature was observed for D_{it} values which was considered as the temperature effects on interface layer's restructuring and the reordering.

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