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Investigation of electrical characteristics of Ag/ZnO/Si sandwich structure

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Abstract
In this study, temperature-dependent current–voltage (I–V), frequency-dependent capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements are carried out for the electrical characterization of a zinc oxide (ZnO) thin film-based diode. The sandwich structure in the form of Ag/ZnO/Si/Al is investigated at temperatures between 220 and 360 K and in the frequency region of 1 kHz–1 MHz. ZnO thin film layer is deposited on a p-Si wafer substrate as a transparent conductive oxide layer by taking into consideration possible electronic applications with intrinsic attractive material properties. At each temperature step, the I–V curves showed about two orders of magnitude rectifying behavior and, according to the Schottky diode relation, the saturation current, zero-bias barrier height and ideality factor were extracted as a function of the temperature. In the case of non-ideal diode characteristics due to the inhomogeneties in the diode as observed from the characteristics of the calculated parameters, effective barrier height values are evaluated. In addition, based on the existence of the interface layer, density of interface states in the band gap region and parasitic resistances were determined by the capacitance measurements.

1 Introduction

In the electronics industry, semiconductor materials have been a subject of interest, and widely used and integrated into device applications [1–3]. In recent years, these materials have been used depending on their functionalities in metal/semiconductor (MS) Schottky diodes and p–n junction formations [1, 4–10]. If there is a layer between the metal and semiconductor, a MS structure changes to metal/oxide/semiconductor (MOS), as such, the results obtained from the current–voltage (I–V), capacitance–voltage (C–V) and conductance–voltage (G/ω–V) measurements deviate significantly from the ideal diode behavior [4, 6, 7]. In this case, the main parameters that affect the performance of MOS diode are predominantly related to the nature and thickness of the interface layer between the metal and semiconductor, surface states formed between the interface layer and semiconductor, series resistance of the diode, and homogeneity of the potential barrier in the MS interface [7, 11, 12]. In other words, the existence of such an interface layer can affect density of the interface states in the band gap region and the main diode parameters such as barrier height, ideality factor and parasitic resistances in the diode [4, 7, 11, 12]. From this point of view, transparent conductive oxide (TCO) thin film structures called wide band gap semiconductors have become topic of interest in the visible region of the solar spectrum for fabrication and also application in a wide variety of transparent electronics [13–15]. In the family of the TCO thin films, zinc oxide (ZnO) is a member of the II–VI semiconductor group [15, 16]. It is an alternative material for electronic applications with intrinsic n-type conductivity, wide band gap and high dielectric constant. In order to realize the knowledge of the rectifying and capacitive characteristics of this film in devices, ZnO based diodes have

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been examined with respect to different ohmic and Schottky metal contacts [9, 17–31]. In these works, as ZnO layer is deposited on TCO film coated glass substrate in the form of MS and deposited on Si substrate in the form of MOS diodes and widely investigated for the purpose of complete device characterization and possible applications in electronic devices. In addition, in these works, the deposition of the ZnO thin film is accomplished with various techniques as molecular beam epitaxy (MBE) [18, 19], vacuum evaporation [22], electrodeposition [23], sol–gel [9, 24, 25, 29], atomic layer deposition (ALD) [30, 31], and sputtering [26]. In the present study, ALD was applied to deposit a ZnO film layer on an Ag/ZnO/Si/Al diode in order to obtain a good and uniform surface coverage with a considerable thickness control [32]. To do this, 5 nm ZnO thin film was deposited on the p-Si/Al substrates by ALD technique at 200 °C that can be treated in low deposition temperature with the aim to obtain high-quality pure materials. The diode structure in the form of Ag/ZnO/Si/Al was investigated in terms of both I–V and C–V characteristics as well as the structural properties of ZnO thin film. It is the case where the performance and stability of an electronic device strongly depend on the characteristics of the interface layer. Based on the experimental temperature-dependent I–V characteristics, the main diode parameters such as saturation current (I_0), zero-bias barrier potential (Φ_{b0}) and ideality factor (n) were evaluated as a function of temperature under forward bias conditions. As a separate attempt in the literature to examine ZnO based diodes, the present work focuses on C–V and G/ω–V characteristics in the frequency range of 1 kHz–1 MHz at room temperature in addition to analyzing I–V characteristics. Our study also extract characteristic parameters including series resistance (R_s) and interface states affecting the device properties. The study on the capacitance and conductance measurements are focused on bias voltage and applied frequency dependent density of interface states (D_{it}) related to the interfacial layer and surface states in the diode and R_s values. The corresponding voltage and frequency dependent values were also calculated according to the high-low frequency capacitance and Hill–Coleman method, respectively. Lastly, to achieve a better understanding the effects of R_s was also obtained from measurements of C–V and G/ω–V plots by applying the Nicollian–Brews method.

2 Experimental details

An Ag/ZnO/Si/Al sandwich device structure is fabricated by the process order of Al metal contact evaporation on the back side of the Si wafer, ZnO thin film deposition on the Si wafer and Ag top metal contact evaporation on the ZnO surface. The schematic diagram of the diode is shown in Fig. 1. In this structure, commercial p-type, 525 µm

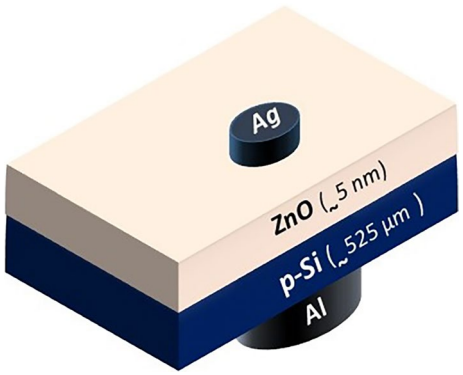

Fig. 1 Schematic diagram of Ag/ZnO/Si/Al device

thick, double-sided polished, monocrystalline with (111) orientation Si wafer having around 1–10 Ω cm resistivity is used as a substrate for the ZnO film layer. Initially, the Si wafer was cleaned by chemical treatment in 10% dilute hydrofluoric acid (HF) solution in order to remove the native oxide layer, rinsed in distilled water and dried under pure nitrogen flow. The back side of the Si wafer was deposited by elemental Al evaporation and then post-annealing treatment was applied at 450 °C using a horizontal Lindberg type furnace under a continuous nitrogen flow to eliminate possible oxidation during annealing. The ZnO thin film layer with 5 nm thickness was deposited on the bare Si surface using a high-vacuum Savannah S300 ALD system. As precursors for the ALD system, diethyl zinc and water vapor were used in the deposition cycles of the ZnO layer at 200 °C substrate temperature conditions with a very slow deposition rate as in the atomic layer-by-layer deposition. As a final step, Ag metal contact deposition was done on the ZnO film surface by means of dot-shaped Cu masks in a 1 mm diameter. Then, 100 °C annealing was applied to the whole diode to improve the adhesion of the room temperature evaporated contacts on the film surface. Structural investigations of the ZnO layer deposited on p-Si surface were detailed by compositional and surface morphological analyses using ZEISS EVO 15 SEM with EDAX detector attachment and analysis of crystalline structure using Rigaku miniflex X-ray diffraction (XRD) system. The fabricated Ag/ZnO/Si/Al structure was characterized by I–V, C–V and G/ω–V measurements between the Ag-top and Al-back contact surfaces. The I–V values were collected using Keithley 2401 source meter in the bias voltage range of ± 2 V. For the temperature dependent measurements at temperatures between 220 and 360 K, a CTI-Cryogenics Model 22 refrigerator system combined with Model SC helium generator was used, and the temperature on the diode was adjusted using a Lakeshore DRC-91C controller. In addition, capacitance measurements were carried out using a Hewlett Packard 4192A

LF model impedance analyzer in the frequency range of 1 kHz–1 MHz at room temperature.

3 Results and discussion

The crystalline nature of the ZnO film on p-type Si substrate was investigated carrying out XRD measurements. As shown in the XRD profile in Fig. 2, ZnO film layer has a polycrystalline nature and any secondary phase contribution is not detected. The diffraction peak is observed at 2θ ~ 33.5° corresponding to the preferred orientation along to (111) direction which indicates the cubic phase is dominant in the structure (JCPDS no. 65-2880). In the compositional analysis of the film, the energy dispersive X-ray spectroscopy (EDS) profile reveals that the relative atomic ratio of Zn and O is about 50:50. In the inset of Fig. 2, surface of the ZnO thin film layer is shown as a two-dimensional SEM micrograph and it is found in the smooth and uniform characteristics as expected from ALD coating [32].

The temperature dependent *I–V* characteristics of the deposited Ag/ZnO/Si/Al structure are presented in Fig. 3 in the temperature interval of 220–360 K. The *I–V* characteristics in each temperature region demonstrate a rectifying nature with a rectification factor in two orders of magnitude.

The current transport through this diode structure is discussed by considering the possible existence of the interfacial layer naturally formed on the Si surface and artificially deposited 5 nm-thick ZnO thin film layer. In this case, the thermionic emission (TE) model can be used to extract the barrier parameters independent of bias voltage as [4, 6, 7, 11];

$$I = I_0\left[exp\left(\frac{qV - IR_s}{nkT}\right) - 1\right] \tag{1}$$

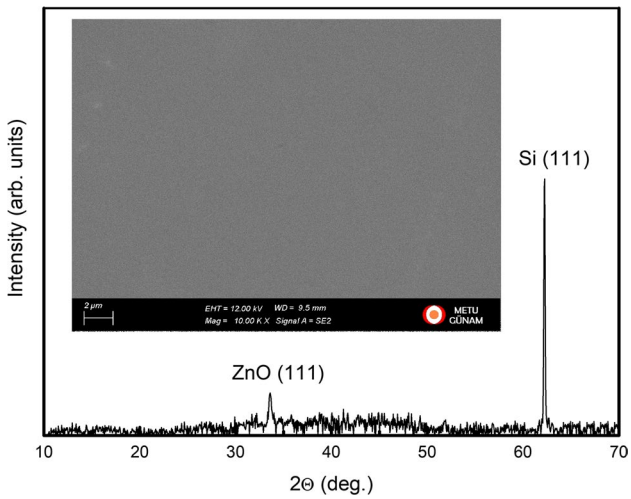

Fig. 2 XRD profile of the ZnO film layer on Si substrate. Inset shows the SEM image of the ZnO film surface

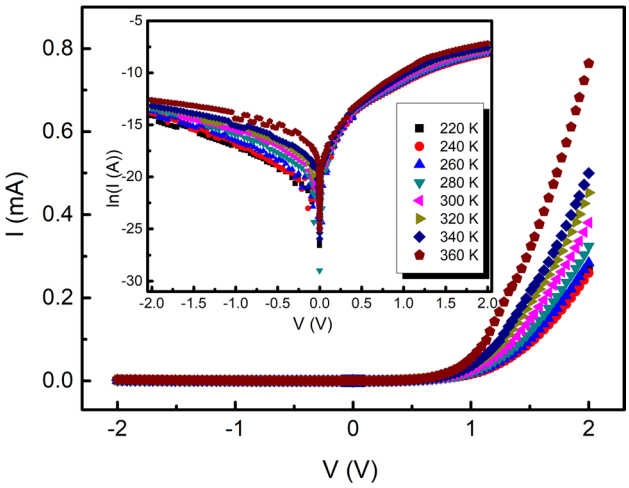

Fig. 3 Temperature dependent I–V characteristics of Ag/ZnO/Si/Al device

where the *I–V* relation is derived under the assumption of $V > 3kT/q$ with eliminating the possible effects of reverse current contribution [4, 7]. In this equation, I is the measured current value under the applied voltage (V), I_0 is the saturation current, q is the electron charge, IR_s term is the voltage drop under the effect of series resistance R_s, n is the ideality factor depending on the current transport mechanism through the junction, k is the Boltzmann constant and T is the temperature of interest. The linear point in the forward bias region is investigated in order to extract the experimental diode parameters with the help of the extrapolated I_0 value derived from the relation,

$$I_0 = AA^*T^{-2}exp\left(-\frac{q\Phi_{b0}}{kT}\right) \tag{2}$$

where A is the effective diode area depending on the metal contact geometry, A^* is the effective Richardson constant of the active layer in the diode and Φ_{b0} is the zero-bias barrier height. At each temperature, the I_0 values are calculated from the zero bias intercept of the linear portion of the forward bias $I - V$ plot (Fig. 3) and tabulated in Table 1. Φ_{b0} values are derived from these experimental results. As can be seen, the values listed in Table 1 and those presented in Fig. 4 are in good agreement with the reported research on sol–gel deposited ZnO thin film [25] and sol–gel deposited nanofiber ZnO thin film [24]. However, they are higher than the estimated value in the epitaxial ZnO layer [18]. This difference could be related to the variation in the structural properties of the ZnO layer deposited using different methods, thus resulting in different characteristics of the interfacial layer and surface states in these device structures.

In the pure TE theory, n is expected to be 1; however, it can be observed greater than this value depending on the

Table 1 The device parameters calculated according to the thermionic emission model given in Eq. 1

T (K)	I_0 (A)	Φ_{b0} (eV)	n
220	4.76×10^{-9}	0.57	4.04
240	9.07×10^{-9}	0.61	3.82
260	1.55×10^{-8}	0.65	3.63
280	2.48×10^{-8}	0.69	3.45
300	3.77×10^{-8}	0.74	3.27
320	5.48×10^{-8}	0.78	3.11
340	7.67×10^{-8}	0.82	2.98
360	1.04×10^{-7}	0.86	2.85

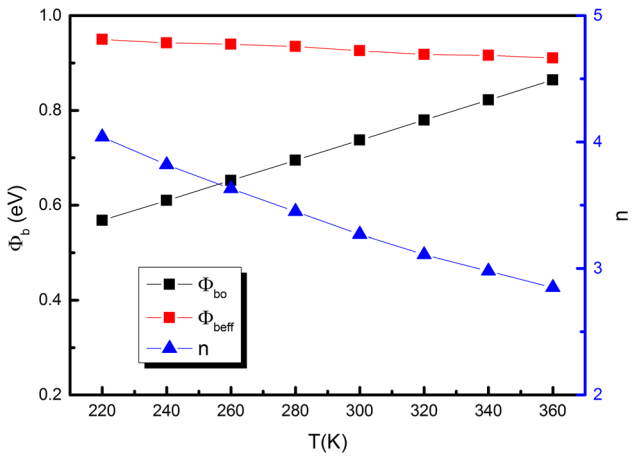

Fig. 4 Variation of Φ_{b0}, Φ_{beff} and n values with temperature for Ag/ZnO/Si/Al device

possible effects of image force lowering even if TE is dominant in the current flow [33, 34]. In addition, the deviation from the ideal TE assumption can be attributed to a variety of dominating influence of conduction mechanism depending on generation–recombination current in the junction region, field emission and anomaly on TE, and tunneling current flow due to the interfacial layer [4, 6, 7, 35, 36]. Thus, n values are determined from the slope of the linear region of the I–V curve with the following relation

$$n = \frac{q}{kT}\left(\frac{dV}{dln(I)}\right) \tag{3}$$

As shown in Fig. 4, the n values have temperature dependent characteristics and are in a decreasing trend with increasing temperature. The calculated values given in Table 1 are in the same range as those reported values in a similar device structure fabricated differently with a ZnO layer as regards structure and deposition techniques [18, 24, 25]. The nature of the non-ideal values in this device and the differences from the reported values could be due to the possible effects of other current transport processes rather than pure TE related to the chemical interactions between the layers, their material characteristics and existence of interfacial layer in the device. Since the diode parameters are derived in the linear forward bias I–V region below saturation, the possible effects of R_s on the voltage drop across the diode structure may have been neglected in the experimental values following Eq. 3. In fact, whereas downward curvature of the forward bias I–V behavior is attributed to the effect of R_s, the diode operation and behavior of carrier in the current flow can be dominated by interface states in both the inversion and depletion regions [37, 38]. The forward bias region is found to be under the effect of interface states apart from R_s in the high forward bias region. On the other hand, the current values in the reverse voltage region demonstrate a slowly increasing behavior without any effect of saturation as shown in Fig. 3. Therefore, this reverse current behavior can be the reason of spatial inhomogeneity in the barrier [39, 40]. As a function of diode temperature, calculated Φ_{b0} values increase whereas n values decrease with increasing temperature. Such variation in these parameters can be related to the deviation from the TE model in current flow under the effect of inhomogeneous distribution of interface states (D_{it}) and Φ_{b0}. The evaluation of Φ_{b0}, using the temperature-dependence of the barrier parameters show non-linearity as observed in the semi-logarithmic plot of I_0 with respect to inverse temperature (plot of $\ln(I_0/T^2)$ vs $1/T$ in Fig. 5). On the other hand, this dependence might be included in the evaluation of this conventional plot, and it could be modified as $\ln(I_0/T^2)$ versus $1/nT$.

As shown in Fig. 5, the temperature dependence of this plot has a linear behavior compared to the plot of $\ln(I_0/T^2)$ versus $1/T$. Therefore, this fact can be considered as indication of the possible tunneling mechanism in carrier conduction from the metal through the oxide interface and into the

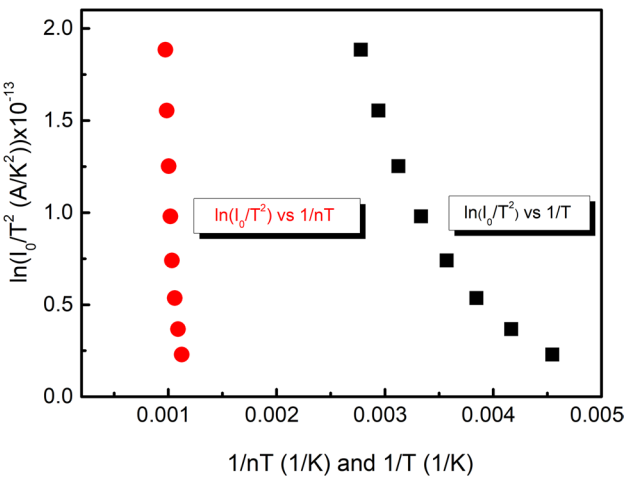

Fig. 5 $\ln(I_0/T^2)$ versus $1/nT$ and $1/T$ plots for Ag/ZnO/Si/Al device

semiconductor layer [39–43]. Under this assumption Eq. 2 can be expressed with the effective barrier height depending on the variation in n with temperature as [34, 40, 44],

$$I_0 = AA^*T^{-2}exp\left(-a\chi^{0.5}\delta\right)exp\left(-\frac{q\Phi_{beff}}{nkT}\right) \quad (4)$$

where $exp\left(-a\chi^{0.5}\delta\right)$ is used in the modified relation (Eq. 4) to discuss the transmission across the interface. The term $a\chi^{0.5}\delta$ is also defined as a tunneling factor with a constant a depending on the tunneling effective mass m^*, χ is the mean tunneling barrier height in the interface layer and δ is the thickness of the layer where tunneling takes place. Therefore, assuming the only interface layer as being the deposited ZnO layer between Ag metal contact and Si, $\alpha\chi^{0.5}\delta$ is approximated as 17.6 according to Eq. 4. The value is obtained without any possible reverse current contribution to carrier tunneling and assuming on the limitation of $V > 3kT/q$ [44]. The effective barrier height Φ_{beff} values are obtained from the modified I_0 expression given in Eq. 4 and presented in Fig. 4 to re-evaluate the experimental values extracted from the TE model. In good agreement with the reported results by Sheng et al. [18], this flat band barrier height approximation can be used to evaluate the I–V characteristics of the diode under the effect of inhomogeneities observed as non-ideal Schottky behavior. As seen in Fig. 4, the calculated effective values are larger than Φ_{b0} values in all temperatures; however, Φ_{beff} values are found to be in direct proportionality with the change in the temperature. Since it has a linear behavior with the temperature, linear Φ_{beff} values can be estimated as

$$\Phi_{beff} = \Phi_b(0\,\mathrm{K}) + \alpha T \quad (5)$$

with the barrier height at 0 K ($\Phi_b(0\,K)$) and negative temperature coefficient of the barrier height (α). From the linear correlation with temperature, the slope of the relation in Eq. 5 gives $\alpha = 3 \times 10^{-4}$ eV/K, and $\Phi_b(0\,\mathrm{K}) = 1.01$ eV which is close to the band gap value of p-Si. The temperature coefficient value, α, is also in very close agreement with the literature for Si [40].

The forward and reverse biased C–V and G/ω–V profiles are given in Fig. 6a and b, respectively. These measurements are carried out in the voltage range from − 1 to + 3 V, and the different frequencies between 1 kHz and 1 MHz at room temperature. As shown in Fig. 6, the experimental values of C and G/ω are in decreasing behavior with increasing frequency due to the effect of the interface states localized at the interface with the possible presence of a native oxide layer on the surface of the Si in addition to the possible effects of the ZnO layer [45]. The observed change in the capacitance values, especially at lower frequencies, can be attributed to the characteristics of density of interface states (D_{it}) in which they can respond to the

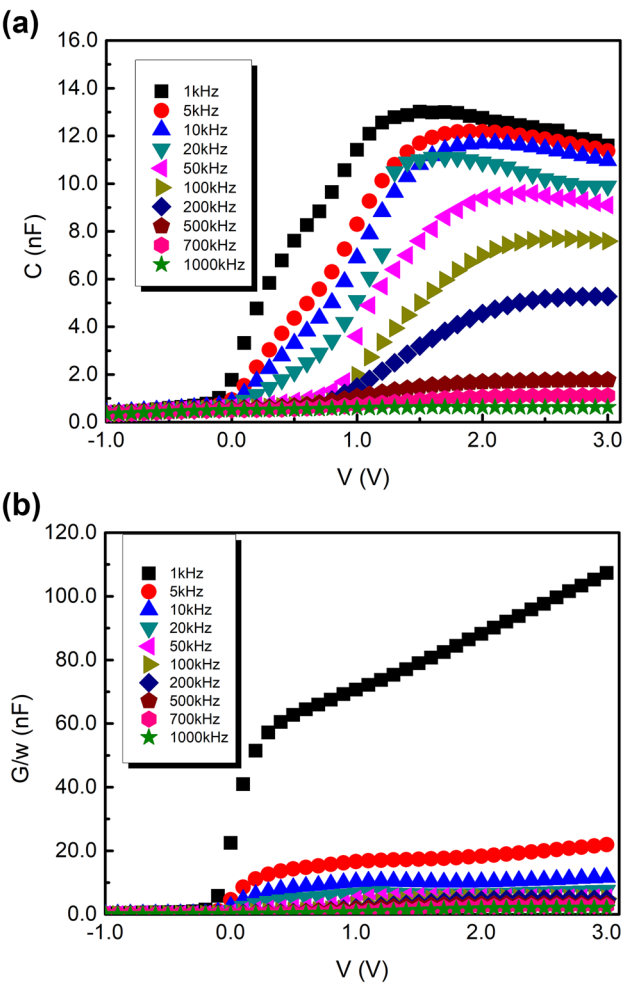

Fig. 6 **a** Frequency dependent C–V and **b** G/ω–V characteristics for Ag/ZnO/Si/Al device

AC signal depending on the applied frequency and the carrier lifetime of charge at these states [45–47].

On the contrary, the increase in frequency values can limit this contribution from the capacitance of the interface states to the total capacitance of the diode. Thus, in the low impedance of the diode, the effect of R_s becomes dominant to the applied voltage as a capacitive behavior [46–48]. This impedance characteristics of the diode under the effect of the oxide layer, D_{it} and R_s can be modeled with an equivalent circuit, where capacitance due to D_{it} (C_{it}) and R_s are in series and totally parallel to the total measured capacitance (C_m), and where interfacial oxide capacitance is in series to this circuit as well. The common way to determine the resistance of the diode as a function of the bias voltage is the admittance method proposed by Nicollian and Brews [46]. Although this approach evaluates the effects of resistance in the whole of the measured range, at sufficiently high frequencies ($f \geq 500$ kHz) and in the strong accumulation region, it can be used to

calculate the R_s values from C_m and G_m measured in this region as

$$R_s = \frac{G_m}{\left(G_m\right)^2 + \left(\omega C_m\right)^2} \tag{6}$$

where ω is the angular frequency with $\omega = 2\pi f$. According to this model, the voltage and frequency dependent results are shown in Fig. 7, and these values are in the same order of magnitude with the literature [18, 24].

As given in Fig. 7, in the reverse voltage region at low frequencies, R_s–V plot shows a peak profile. The R_s values have peak depending on frequency in the voltage range from 0 to − 0.2 V, whereas the magnitude of the peak decreases with increasing frequency and at high frequency region it disappears. This decrement of the calculated R_s values with increasing frequency can be attributed to the charges from the interface, fixed oxide, oxide-trapped, and mobile oxide states depending on variations in the voltage and frequency [47–52]. In the same plot as another point of view, the frequency dependent values are in decreasing behavior with increase in the bias voltage and this relation is similar for each frequency profile at different voltages. This could be the indication of different R_s values at each applied voltage and frequency value due to the possible effect of D_{it} at the interface [46, 47].

For this type of device structure with an oxide layer, D_{it} can be related to the net charge state of the oxide film or charge carriers accumulated on the surface of the semiconductor layer. Under the assumption that all interface states are in equilibrium with the semiconductor, the D_{it} values can be expressed as [44, 53],

$$n(V) = 1 + \frac{\delta}{\epsilon_i}\left[\frac{\epsilon_s}{W_D} + qD_{it}\right] \tag{7}$$

with width of space charge region, W_D and the permittivity of the interface and semiconductor layers ϵ_i and ϵ_s, respectively [44, 45]. In addition, the energy of the interface states (E_{it}) in a p-type semiconductor referenced with the bottom of the conduction level is given by [7],

$$E_{it} - E_v = q\Phi_e - qV \tag{8}$$

where Φ_e is the voltage-dependent barrier height effective with the possibility of interface states in the structure. According to Eq. 8, the density distribution curves of the interface states for different applied temperatures are obtained. The D_{it} values as a function of $E_{it} - E_v$ are given in Fig. 8a and the variation with the temperature appears in Fig. 8b.

As shown in Fig. 8b, there is a decrease in the D_{it} values with using temperature. The maximum value obtained at 360 K is 7.9×10^{13} eV^{-1} cm^{-2}, whereas at 220 K it decreases to 6.8×10^{13} eV^{-1} cm^{-2}. This result can be related to the temperature effect on the contacts between metal and

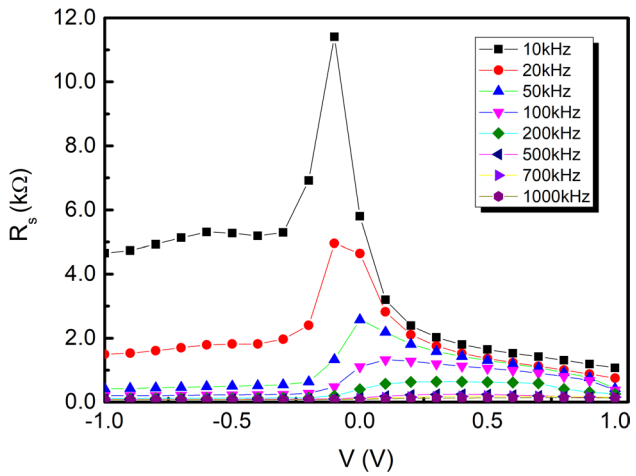

Fig. 7 Frequency dependent R_s versus V plots for Ag/ZnO/Si/Al device

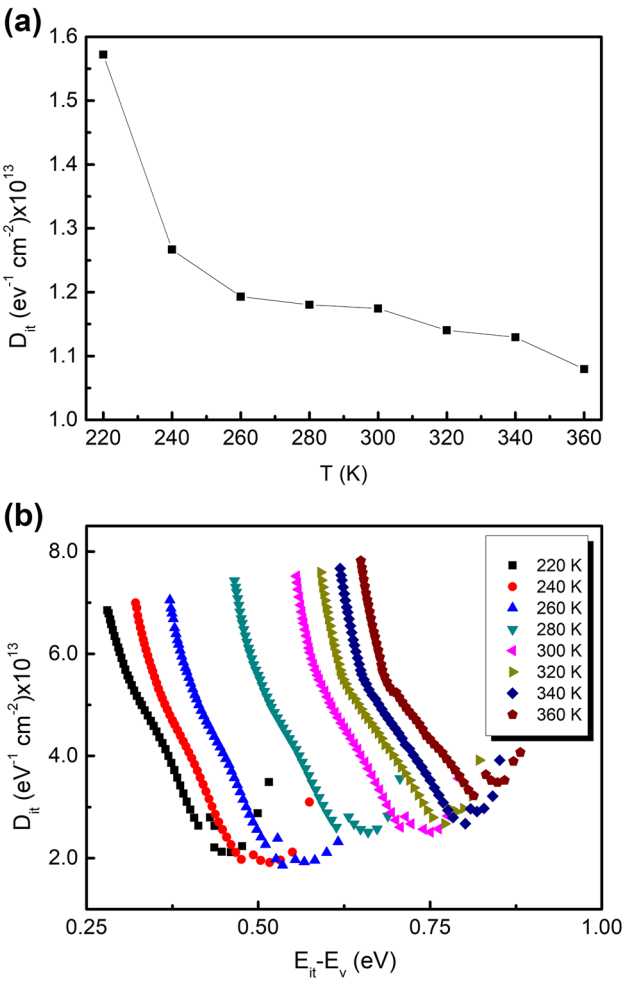

Fig. 8 **a** D_{it} versus $E_{it} - E_v$ plot and **b** D_{it} values with respect to T obtained from $I - V$ analysis

semiconductor via the interface layer [45, 46, 48]. In addition, the D_{it} curves show an exponential behavior with temperature that has a minimum point and a shift toward the valence band due to the existence of interfacial layer and its structural variation depending on the temperature [54]. The obtained range of D_{it} values is close to those extracted for the diode fabricated by nanofiber ZnO film [24].

According to the connection between the surface potential and the applied voltage, coupled with the effect of the AC signal in the junction, the energy distributions of D_{it} can be derived as a function of the applied voltage from equivalent circuit model [55]. Because of the response of the interface states to the AC signal at lower and higher frequencies, high-low frequency capacitance values can be inserted as

$$D_{it} = \frac{2}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}\right] \quad (9)$$

where C_{ox} is the capacitance of the oxide layer that is in direct relation with the dielectric constant of the ZnO layer [56]. In this equation, the bias variation of D_{it} values can be calculated using the measured capacitance values at the highest and lowest frequency, C_{HF} (1 MHz) and C_{LF} (50 kHz), respectively. The obtained energy distribution profiles of the D_{it} values derived from the approximated C_{ox} value as 3.0×10^{-7} F are given in Fig. 9a with a peak over the band gap energy of Si.

In addition, the approximation for peak interface state density correlated with interface state admittance proposed by Nicollian–Goetzberger can be used to determine the D_{it} values and their distribution profile depending on the applied frequency. According to this single-frequency conductance approximation based on Hill–Coleman method, these values can be determined as

$$D_{it} = \frac{2}{qA}\left[\frac{G_{m,max}/\omega}{\left(G_{m,max}/\omega C_{ox}\right)^2 + \left(1 - C_m/C_{ox}\right)^2}\right] \quad (9)$$

where $G_{m,max}/\omega$ corresponds to the measured maximum value in the G/ω–V plot and C_m is the measured capacitance related to $G_{m,max}/\omega$ [57]. Figure 9b shows the variation of the obtained D_{it} values with frequency which decrease as frequency increases. This behavior corresponding to change in frequency can be related to the absence of capacitance contribution of interface states in the high frequency region.

4 Conclusion

In this paper, electrical characteristics of the fabricated Ag/ZnO/Si/Al diode were investigated in order to extract the main diode parameters, detail the dominant current transport

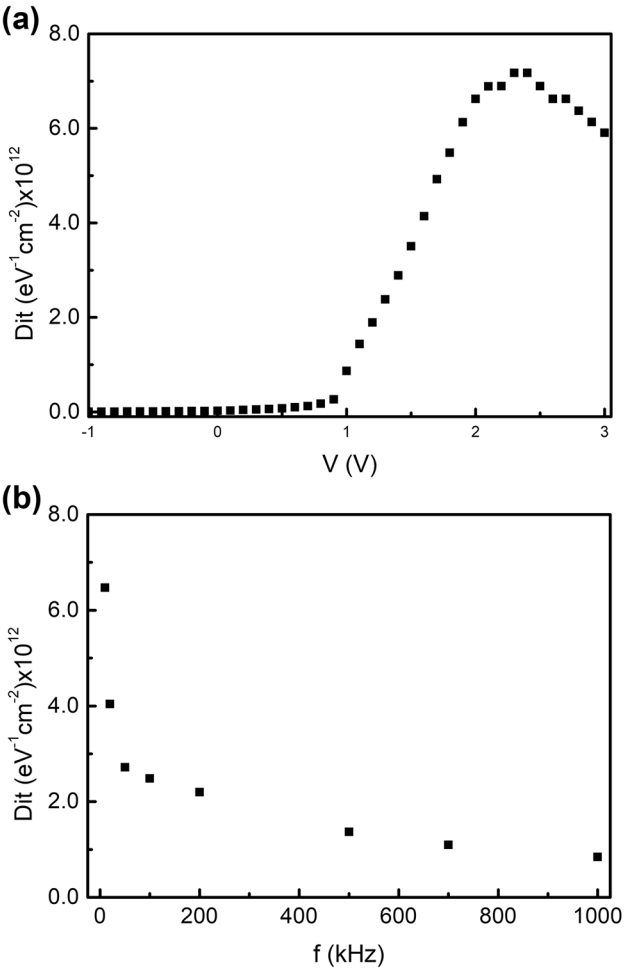

Fig. 9 **a** The variation of D_{it} as a function of V and **b** as a function of f

mechanism through a barrier and the nature of barrier formation in the structure using I–V, C–V and $G/\omega - V$ measurements. From the forward bias region, the Φ_{b0} and n values were determined as a function of temperature in the range of 220–360 K. The room temperature Φ_{b0} in the value of 0.74 eV was found in the interval of reported values given in the literature, whereas n value 3.27 is different from the diodes with a ZnO layer depending on the structure and deposition techniques. On the other hand, both parameters showed non-ideal variations with temperature, and with the contribution of n, Φ_{beff} values were calculated to identify the effect of interface layer in the diode and it appeared as about 0.93 eV at room temperature. According to the temperature-dependence of the diode parameters, TE model was modified with the effects of tunneling current and barrier inhomogeneity in the diode. The R_s values were found in the order of a few kΩ with a peak value at low-frequency using a frequency-dependent profile. However, under the effect of increasing frequency values, the magnitude of the peak

decreases and, then, at the high frequency region disappears from the profile related to the charge characteristics in oxide states depending on variations in the voltage and frequency. In addition, the D_{it} values calculated from these measurements in the range of 2 to 8×10^{12} eV^{-1} cm^{-2} depending on both frequency and bias voltage. These values were found to be in a good agreement in terms of order of magnitude, however, they were observed in decreasing behavior with the increase in the frequency. Furthermore, a similar variation with temperature was observed for the existence of an interfacial layer and its structural variation depending on the temperature.

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