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Frequency effect on electrical and dielectric characteristics of In/$Cu_2ZnSnTe_4$/Si/Ag diode structure

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Abstract
In/$Cu_2ZnSnTe_4$/Si/Ag diode structure was fabricated by sputtering $Cu_2ZnSnTe_4$ (CZTTe) thin film layer on the Si layer with In front contact. The frequency dependent room temperature capacitance and conductance measurements were carried out to obtain detailed information of its electrical characteristics. Admittance spectra of the diode exhibited strong frequency dependence and the obtained values showed decreasing behavior with the increase in the applied frequency. The effect of interfacial film layer with series resistance values and density of interface states were investigated by taking into consideration of non-ideal electrical characteristics of the diode. The distribution profile of the interface states was extracted by Hill-Coleman and high–low frequency capacitance methods. As a function of frequency, they were in proportionality with the inverse of applied frequency. Dielectric constant and dielectric loss parameters were calculated from the maximum value of the diode capacitance at the strong accumulation region. The loss tangent showed a characteristic peak behavior at each frequency. Based on the time-dependent response of the interfacial charges to the applied ac field, the values of ac electrical conductivity and complex electric modulus were calculated and discussed as a function of frequency and bias voltage.

1 Introduction

In recent years, several studies have been carried out on thin film technology mainly as oxide, dielectric and semiconductor layers due to their wide range applications in Schottky barrier and semiconductor p–n diodes [1–6]. In the fabrication and application of these types of diode structures, electrical characteristics of the constituent materials, parasitic resistances in the diode and interfacial properties have been investigated to determine their dominant effects on device performance [7, 8]. In most cases, depending on the material characteristics, effects of the film layer deposition and also native and/or artificial layer on the surface of the semiconductor layer, current flow and admittance characteristics can deviate from the ideal case [7]. In this case, possible inhomogeneities is mainly occurred in the diode structure with the interface states in barrier height formation and series resistance effect on the current flow from the top to back contacts.

Due to the industrial demand in these types of device applications, thin film technology has been developed on chalcopyrite thin films due to their favorable optical and electrical properties. Among these film structures, CdTe is one of the most popular thin film layers in heterojunction diodes. Apart from being presented as a promising absorber layer in photovoltaics, its ternary alloys, CdZnTe and HgCdTe are the ones in detector applications. However, there are limited works on Te-based thin film compounds and they have been less studied than their sulphide and selenide counterparts [9–14]. Recently, I_2–II–IV–VI_4 kesterite structures can be found at the center of various technological interests with including earth-abundant, low-cost and non-toxic elements for several opto-electronical applications [15–17]. In the search for an environment-friendly

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and low-priced material, these quaternary compounds have been employed to tune their electronic characteristics for the possible diode applications. Among these compounds, Cu_2ZnSnS_4, $Cu_2ZnSnSe_4$ and $Cu_2ZnSn(S,Se)_4$ have attracted a prominent attention due to the similarities in the crystal structure and electronic characteristics with well-known chalcopyrite compounds such as $CuInSe_2$ and $Cu(In,Ga)Se_2$ [18–22]. In addition to tunable physical properties by changing chemical composition of the constituent elements, their promising characteristics such as direct band gap of about 1.5 eV, high optical absorption behavior with absorption coefficient up to $10^5 cm^{-1}$ and p-type conductivity make them favorable in electric and opto-electric applications [20–23]. In fact, these kesterite structures are analogous to $Cu(In,Ga)Se_2$ by substituting the rare metals, In and Ga by Zn and Sn and trigger significant attention as being a low-cost and environmental friendly alternative to the conventional photovoltaic materials [24]. As a subject of research and potential applications, $Cu_2ZnSnTe_4$ (CZTTe) is expected to be similar to compound with S and Se. Therefore, it has been employed to offer an extensive field for Te-based material design [12]. In fact, among the Cu_2ZnSnX_4 (X = S, Se, Te) group of compounds, the distribution of Cu, Zn and Sn can cause negligibly small differences in the material properties mainly as band structures, electronic characteristics and Te contribution is expected to present similar characteristics to the structure similar to S- and Se-based compounds [10].

Under the aim of triggering the efforts on the new materials for commercially competitive kesterite thin film alloys, this Te-based compound was fabricated considering its sulphide and selenide counterparts. In the previous work, the authors presented the temperature dependent electrical characteristics of In/CZTTe/Si/Ag diode in which quaternary CZTTe thin film layer deposited by DC/RF sputtering using stacked precursors on one-sided polished n-Si wafer substrate by taking into account of the presence of interfacial layer and possible dominant current transport mechanisms [25]. Because Si is the most well-known semiconductor for manufacturing electronic devices, fabrication on Si-layer can present advantages on the physical and technological properties in diode applications with its historical background. The total current flow through the diode was modelled by defining Gaussian distribution on the formation of barrier height. Inhomogeneous barrier height formation depending on the presence of the interfacial layer and non-uniformity of the interfacial charge distribution were discussed. Due to the requirement to have the complete knowledge of carrier dynamics under the effect of interface states, in this work, capacitance and conductance characteristics of this fabricated diode were investigated. In fact, the formation of the film layer and possible effects of interface state density and series resistance showed the considerable variations on the performance and reliability of these structures. Therefore, capacitance–voltage (C–V) and conductance-voltage (G/ω–V) properties of the diode was determined to figure out the effects of this film layer in the diode structure and the nature of interface states in a wide range of frequency.

1.1 Experimental details

In this study, mono-crystalline n-type Si (111) wafer having the resistivity 5–10 (Ω cm) was used as a substrate layer and back metal contact on this layer was formed by elemental Ag evaporation onto the whole back surface for electrical measurements. Subsequently, Si wafer was annealed at 400 °C to form a low resistive Ag back contact. Following to this process, 400 nm thick CZTTe thin film layer was deposited on this layer at about 200 °C substrate temperature using three magnetron DC/RF sputtering system with sequential sputtering of Cu, SnTe and ZnTe targets. Thin film deposition process was carried out at a chamber pressure of about 6×10^{-3} Torr with pure Ar gas flow of 6 sccm and thickness of each thin film layer was controlled by Inficon thickness monitor. X-ray diffraction (XRD) measurements were performed by Rigaku miniflex XRD systems. Almost stoichiometric film layer was found in polycrystalline structure with the main orientation along (112) plane direction. The diode structure was completed by thermal evaporation of 100 nm thick *In* metal contact on the film layer in 2 mm diameter circular geometry. The fabricated diode was annealed at 100 °C to increase the adhesion of the contacts to the film surface. For the electrical analysis, room temperature C–V and G/ω–V measurements were carried out in a wide frequency range from 50 kHz to 10 MHz by using computer controlled Hewlett Packard 4192A LF model impedance analyzer.

2 Results and discussion

The variations of the capacitance (C) and conductance (G/ω) with bias voltage (V) at different frequencies of the fabricated diode as shown in Fig. 1a and b were investigated under the possible effects of the interface states and parasitic resistances in the structure.

The admittance characteristics of the fabricated diode were analyzed under the assumption of the deviation from ideal capacitive behavior due to interface capacitance contribution as a possible effect of interface states to the electrical characteristics of the diode. As seen in this figure, obtained C and G/ω values as a function of V are sensitive in the forward bias region at low frequencies. The values of C and G/ω decrease as the applied frequency decreases, especially in the depletion region, due to the effects of ac signal on trap states [27–29]. At low frequencies, increase in the experimental values can be related to the existence of interface states in the diode structure. Hence, it can be the

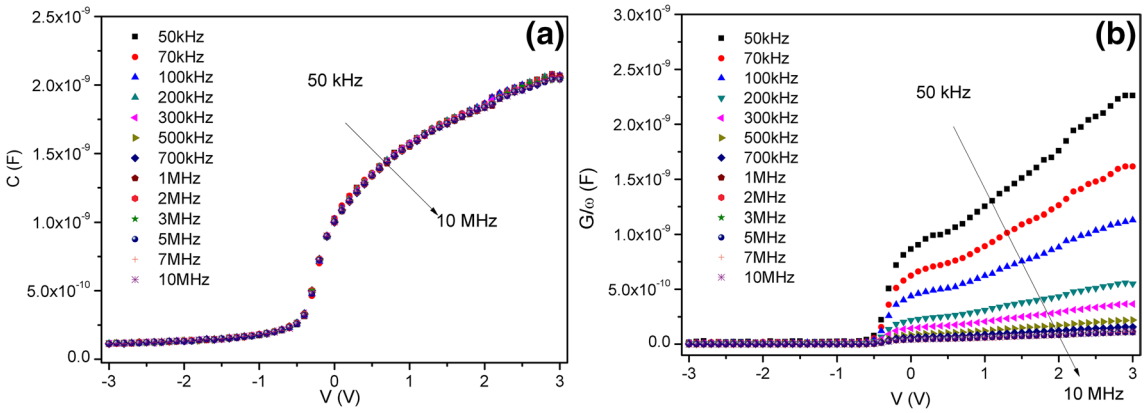

Fig. 1 Frequency dependent**: a** *C–V* and **b** $G/\omega-V$ characteristics of In/CZTTe/Si/Ag diode at room temperature

indication of the effects of interfacial space charge formation in this region [30]. The higher values of C at low frequencies are attributed to the excess capacitance resulting from the density of interface states (D_{it}) which is in equilibrium with the semiconductor that can follow the ac signal. In fact, D_{it} can easily follow the applied signal at this frequency range and contribute to the capacitive response of the diode in which this behavior can vary with the applied frequency and also intrinsic characteristics of the interface states as relaxation time of charges. The interface layer can show an electrochemical reaction to the applied electric field, and it can be polarized with displacing the charges at the interface states from their equilibrium [31, 32]. Therefore, interface state charges affect the observed capacitive behavior with polarization depending on their time-dependent response. On the other hand, under the effect of high frequencies, this contribution to the total capacitance occurs in a negligible small amount since the charges cannot follow ac signal at this range. The observed non-ideality behaviors in the admittance spectra can be due to inhomogeneities in the interfacial layer and barrier height in the diode. In this case, R_s and D_{it} become considerably significant characteristic parameters in the analysis of the origin of the frequency dispersion in these characteristics [28]. Considering basic equivalent circuit model, the diode can be assumed to be under the effects of interface states with associated capacitance (C_i) and resistance (R_i), and also R_s. Due to the metal and rectifying contact formation (and/or contact interfaces) and deviation from uniformity in the diode active layers, R_s could be related with the changes in the electrical properties of diode structure [8, 33]. Although these values were reported in the previous work depending on the change in the diode temperature, the frequency dependent characterization is also important to get accurate and reliable results [8, 34, 35].

According to the admittance method on the analysis of R_s [8], voltage dependent real values can be observed from the obtained spectra of the diode in Fig. 1 at sufficiently high frequencies and in the strong accumulation region. In this region, the maximum value of the diode capacitance can be related to the additional layer capacitance, voltage and frequency dependence of R_s values that can be calculated as [7, 8],

$$R_s = \frac{G}{G^2 + (\omega C)^2} \tag{1}$$

where ω is the angular frequency of the applied electric field and related to the applied frequency as $\omega = 2\pi f$. From $C-V$ and $G/\omega-V$ measuremens, obtained R_s values as a function of bias voltage in various frequencies are shown in Fig. 2 together with the values as a function of frequency shown in the inset. As seen from this figure, R_s values were obtained in the same order of magnitude that was calculated from *I–V* measurements in the previous work [25]. In addition, the calculated values strongly depend on frequency and voltage; they showed decreasing behavior with the increasing applied bias voltage at each frequency. This observed behavior depending on the change in both voltage and frequency can be attributed to the interface layer and the distribution of D_{it} [36]. In order to detail electrical quality of the interface, D_{it} values was calculated as a function of frequency. According to the Hill-Coleman conductance method, D_{it} can be formulated as [37],

$$D_{it} = \frac{2}{qA}\left(\frac{(G/\omega)_{\max}}{\left((G/\omega)_{\max}C_i\right)^2 + \left(1 - C/C_i\right)^2}\right) \tag{2}$$

where q is the electrical charge, A is the active area of the diode, G is the measured conductance and notation of *max* in subscript denotes its maximum, C is the capacitance value corresponds to this maximum value, and C_i is the capacitance in the accumulation area related to the capacitance effect due to the interfacial layer formulated in the strong accumulation region as [38];

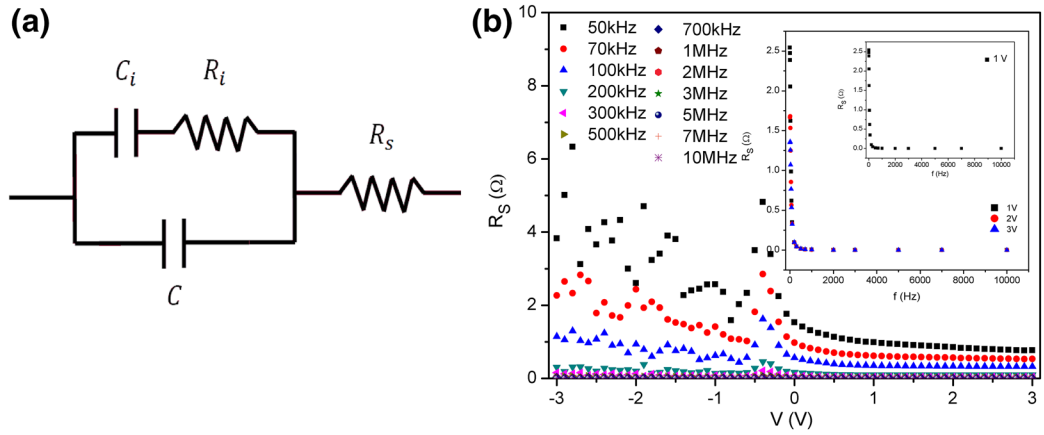

Fig. 2 Frequency dependent R_s values of In/CZTTe/Si/Ag diode at room temperature

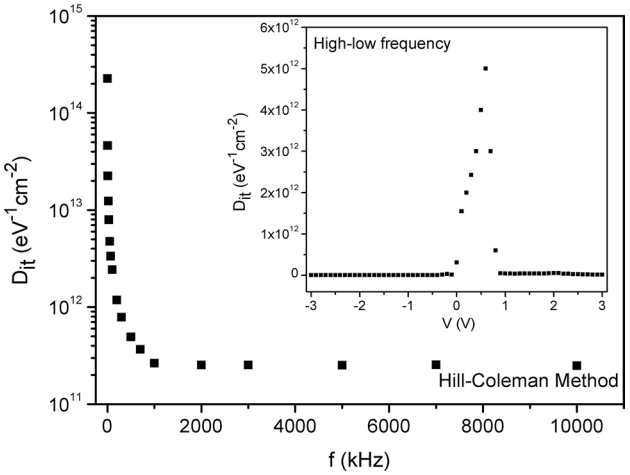

Fig. 3 D_{it} characteristics of In/CZTTe/Si/Ag diode in terms of Hill-Coleman and high-low frequency capacitance ($C_{HF} - C_{LF}$) methods (inset)

$$C_i = C\left(1 + \left(\frac{G}{\omega C}\right)^2\right) \tag{3}$$

The distribution profile of the calculated D_{it} values is shown in Fig. 3 with the variations in frequency and they were observed in a decreasing behavior with the increase in the applied frequency. This fact can be the result of the interface state response to the applied ac signal in high frequency region [39]. Moreover, bias voltage dependent distribution of D_{it} values was calculated from the high–low frequency capacitance ($C_{HF} - C_{LF}$) method as [40, 41],

$$D_{it} = \frac{C_{it}}{qA} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1}\right] \tag{4}$$

where C_{HF} and C_{LF} are the measured highest frequency capacitance (for this study at 1 MHz) and lowest frequency capacitance (for this study at 50 kHz), respectively. The experimental results on the voltage dependence of D_{it} values were given in the inset of Fig. 3. As seen from figure, a peak observed at around 0.65 V in the depletion region can be the indication of interfacial states due to the interruption of the periodic lattice at the surface of the structure [42].

Based on the experimental C and G/ω values, capacitive and conductive nature of the materials can be detailed by the dielectric analysis. The dielectric behavior of the diode was investigated based on the complex dielectric constant (ε^*), ac electrical conductivity and complex electric modulus (M^*) in the wide frequency range from 50 kHz to 10 MHz at room temperature. Considering the effect of interfacial layer in the capacitive behavior of the diode structure, the complex formalism of ε^* can be expressed as;

$$\varepsilon^* = \varepsilon' - \varepsilon'' \tag{5}$$

where ε^* is also known as a permittivity of a structure relative to that of the permittivity of a vacuum, ε_0 with its real and imaginary parts ε' and ε'', respectively [43]. These frequency dependent components correspond to the dielectric constant and dielectric loss of material relating to the energy storage and loss in the diode under the applied electric field, respectively [31]. In the case of the strong accumulation region, the maximum value of the diode capacitance corresponds to the insulator capacitance and therefore ε' can be derived from the relation as $C = \varepsilon' C_0$, where C_0 is the equivalent capacitance of an empty space. Similarly, at the same bias region, ε'' can be calculated using the experimental conductance values as $G/\omega = \varepsilon'' C_0$. [35]. Therefore, these components were extracted from the measured C and G/ω values at the strong accumulation region as [44, 45],

$$\varepsilon' = \frac{C}{C_0} = \frac{Cd_i}{\varepsilon_0 A} \tag{6}$$

and

$$\varepsilon'' = \frac{C}{\omega C_0} = \frac{Cd_i}{\omega \varepsilon_0 A} \tag{7}$$

where C_0 can be expressed with diode active area, A and interfacial layer thickness, d_i as $C_0 = \varepsilon_0 A/d_i$. At various frequencies, the obtained values of ε' and ε'' are presented in Fig. 4 as a function of applied bias voltage.

The calculated frequency dependent ε' and ε'' values are shown in Fig. 4 and these values were found in decreasing behavior with increase in frequency at each voltage, whereas ε' shows a frequency independent nature in the negative voltage region. Since C and G/ω were sensitive to the interface properties and also there is a considerable effect of parasitic resistances on these values, this inverse relation could be explained with the change in the response time of the interfacial dipole orientation to the applied ac field [46, 47]. The increase of the capacitance with the contribution of charge carriers localized at the interface states depends on the ability of them to follow the applied ac signal [25, 26, 33] and so that these carriers can hop between these states which have different dipole orientations. However, at high frequency values, the charges acting a role in this polarization could not have enough time to relax in equilibrium and react to the applied ac field [31, 47]. Therefore, the observed variations in ε' and ε'' with frequency shown in Fig. 4 can be the indication of the dispersion behavior due to the inhomogeneity in the diode with the effect of accumulation of the charges at the boundary of less conducting regions and interfacial polarization [28, 43, 44].

In addition, the ratio of ε' and ε'' is related to the efficiency of a capacitive behavior of the interfacial material and energy losses in the diode, this parameter is defined in radian as a dissipation factor or loss tangent (tan δ) as [38],

$$\tan\delta = \frac{\varepsilon''}{\varepsilon'} = \frac{G}{\omega C} \tag{8}$$

The frequency response of obtained tan δ values and the characteristics of tan δ with a peak behavior at each frequency are shown in Fig. 5. This observed behavior can be related to the frequency dependence of ε' and ε'' values. Furthermore, D_{it}, R_s of the diode, and d_i of the interfacial layer can be responsible for this behavior of *tanδ* [35, 46]. The variations in permittivity and the resulted tan δ profiles with frequency were found to be strongly depending on the applied voltage in certain frequency regions. In this respect, at low frequencies, these frequency dependent profiles can be the indication of the presence of possible polarization processes as electronic, ionic, dipolar, and interfacial or surface polarization and they may contribute to the values of these derived quantities [31, 46, 47]. Moreover, as a result of the fact that D_{it} can not follow the ac signal at high-enough frequencies (f ≥ 500 kHz) and the interfacial contributions become ineffective. Therefore, in this region ε' values was

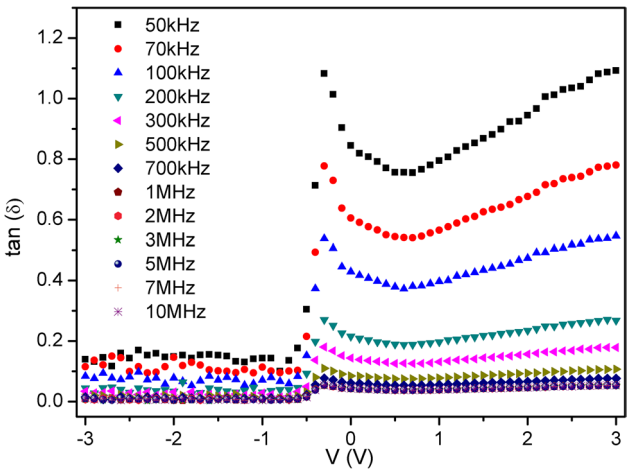

Fig. 5 Frequency dependent tan δ values of In/CZTTe/Si/Ag diode at room temperature

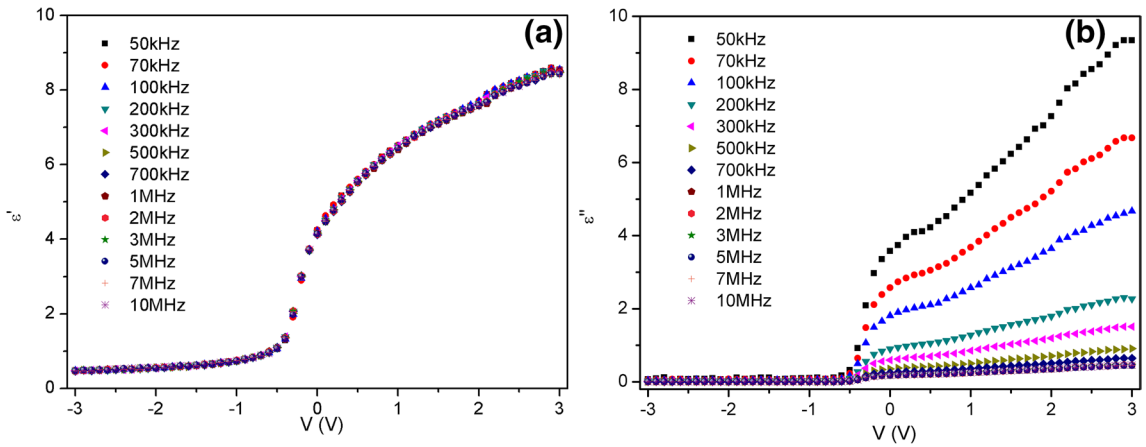

Fig. 4 Frequency dependent: **a** ε' and **b** ε'' values of In/CZTTe/Si/Ag diode at room temperature

observed closer to ε'' values and their ratio, tan δ values were in linear behavior [46]. This profile of tan δ with frequency can be attributed to re-structure and re-ordering of interface states under ac field [28, 48, 49].

The inhomogeneity in the fabricated diode structure can be related to the electrical conductivity in which the charges is expected to accumulate at the regions near to the less conductive boundaries [31, 50] and this dispersion of ac electrical conductivity (σ_{ac}) due to the localized accumulation at the grain boundaries of dielectric material can be written as [38, 51],

$$\sigma_{ac} = \omega C_m \tan\delta\left(d_i/A\right) = \omega\varepsilon_0\varepsilon'' \tag{9}$$

In general, it is known that dc conductivity is expected to be directly related to the applied frequency depending on only the dielectric loss. As given in Fig. 6, the calculated σ_{ac} values were in increasing behavior with increasing frequency [19, 52, 53]. The increase in these experimental values can be connected with an increase of the eddy current and it is also related to the increase of tan δ [54]. This behavior can also be attributed to a gradual decrease in the R_s values with increasing frequency [5, 28, 46, 54].

The complex impedance (Z^*) and complex electric modulus (M^*) were used to describe the dielectric properties in detail. In fact, it is an alternative approach to identify the effect of interfacial layer in the electrical characteristics of the diode by considering the possible carrier conduction mechanisms, polarization and relaxation responses [55, 56]. Analysis of ε^* within these formalisms is commonly used to separate the bulk and the surface phenomena and to determine the bulk dc conductivity of the material [35] According to the Z^* in the expression of $Z^* = 1/i\omega C_0\varepsilon^*$, as a simply geometric inverse of the ε^*, M^* can be defined as,

$$M^* = i\omega C_0 Z^* \tag{10}$$

where real and imaginary part of M^* are related to ε^* as $M' = \varepsilon'/(\varepsilon'^2 + \varepsilon''^2)$ and $M'' = \varepsilon''/(\varepsilon'^2 + \varepsilon''^2)$, respectively [28, 31, 43]. The frequency dependences of these modulus values at different voltages are shown in Fig. 7 where with the voltage dependent plots are given in the inset. From these profiles, both of these parts of M^* were found to be sensitive to the variations in frequency. In fact, the observed spectra of ε' and ε'' shown in Fig. 4 are the indication of such frequency and voltage dependent profiles of M^*. The observed inverse dependence to the frequency can be explained by the contribution of the interface trap charges [28] and Fig. 7 inset shows that the change in the bias voltage does not dominant than the frequency effect in the values of M' and M''.

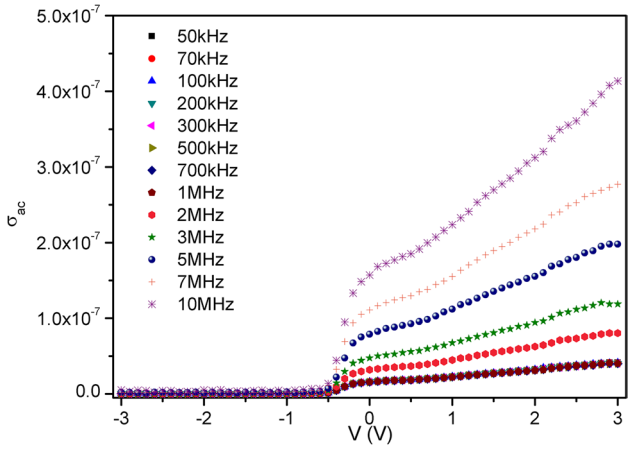

Fig. 6 Frequency dependent σ_{ac} values of In/CZTTe/Si/Ag diode at room temperature

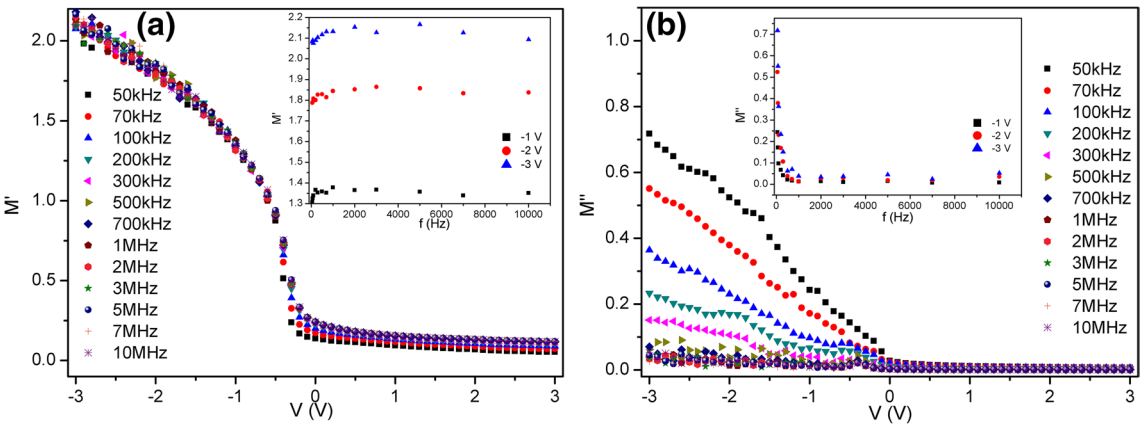

Fig. 7 Frequency dependent: **a** M' and **b** M'' values of In/CZTTe/Si/Ag diode at room temperature

3 Conclusion

In this work, frequency effects on the capacitance and conductance behaviors of In/CZTTe/Si/Ag diode structure were analyzed. In addition to the temperature dependent *I–V* analysis reported in the previous work, the electrical and dielectric characteristics of the fabricated diode structure were investigated in a wide range of frequency from 50 kHz to 10 MHz at room temperature in the voltage range from -3 to 3 V. The non-idealities in admittance spectra of the diode were explained by the possible effect of R_s with the contribution of inhomogeneity in the formation of barrier height and capacitive responses of interface states. R_s values were obtained in the same order of magnitude as in the authors' previous work and these values were found in decreasing behavior with the increasing applied bias voltage at each frequency. The frequency and voltage dependent distribution of D_{it} values were extracted by Hill-Coleman and $(C_{HF} - C_{LF})$ methods. Decrease in the values of ε' and ε'' depending on increase in the applied frequency was attributed inhomogeneity in the diode with the effect of accumulation of the charges at the boundary of less conducting regions and interfacial polarization. This observed fact on interfacial space charge formation and response to the applied ac field was accompanied with the change in ac conductivity σ_{ac} and M' and M''. It was concluded that the obtained dielectric parameters were in a strong function of frequency and bias voltage depending on their time-dependent response of interface state charges to the capacitive behavior with polarization processes.

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