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ARTICLE

# Investigation of carrier transport mechanisms in the Cu–Zn–Se based hetero-structure grown by sputtering technique[1]

H.H. Güllü, M. Terlemezoğlu, Ö. Bayraklı, D.E. Yıldız, and M. Parlak



**Abstract:** In this paper, we present results of the electrical characterization of n-Si/p-Cu–Zn–Se hetero-structure. Sputtered film was found in Se-rich behavior with tetragonal polycrystalline nature along with (112) preferred orientation. The band gap energy for direct optical transitions was obtained as 2.65 eV. The results of the conductivity measurements indicated p-type behavior and carrier transport mechanism was modelled according to thermionic emission theory. Detailed electrical characterization of this structure was carried out with the help of temperature-dependent current–voltage measurements in the temperature range of 220–360 K, room temperature, and frequency-dependent capacitance–voltage and conductance-voltage measurements. The anomaly in current–voltage characteristics was related to barrier height inhomogeneity at the interface and modified by the assumption of Gaussian distribution of barrier height, in which mean barrier height and standard deviation at zero bias were found as 2.11 and 0.24 eV, respectively. Moreover, Richardson constant value was determined as 141.95 $Acm^{-2}K^{-2}$ by means of modified Richardson plot.

*Key words:* Schottky barriers, junction diodes, surface and interface states, thermionic emission, sputtering.

**Résumé :** Nous présentons ici les caractéristiques électriques d'une hétéro-structure n-Si/p-Cu–Zn–Se. Nous trouvons que le film pulvérisé a un comportement riche en Se, de nature poly-cristalline tétragonale, avec orientation privilégiée (112). Nous mesurons une bande interdite de 2,65 eV pour les transitions optiques. Les mesures de conduction indiquent un comportement de type p et le mécanisme de transport de porteur est modélisé selon la théorie d'émission thermoïonique. Les caractéristiques électriques de cette structure sont déterminées à l'aide de mesures courant–voltage dépendants de la température, dans le domaine 220–360 K et à température de la pièce et à l'aide de mesures des caractéristiques capacitance–voltage et conductance–voltage. L'anomalie dans les caractéristiques courant–voltage est reliée à l'inhomogénéité de la hauteur de barrière à l'interface et modifiée par l'hypothèse d'une distribution gaussienne de hauteurs, dans laquelle une hauteur moyenne de barrière et une déviation standard sont trouvées à polarisation nulle avoir valeur de 2,11 et 0,24 eV respectivement. De plus, nous utilisons le graphique modifié de Richardson pour déterminer la constante de Richardson comme étant 141,95 $Acm^{-2}K^{-2}$. [Traduit par la Rédaction]

*Mots-clés :* barrière de Schottky, diode à jonction, états de surface et d'interface, émission thermoïonique, pulvérisation.

## 1. Introduction

Recently, there has been intense attention on semiconducting material to reach for high efficiency solar energy conversion [1, 2]. In the thin film photovoltaic applications, the solar industry mostly depends on cadmium (CdTe) and chalcopyrite compounds, such as $CuInSe_2$ (CIS) and $CuGaInSe_2$ (CIGS), which become a preferabe choice to traditional crystalline silicon wafers [2]. On the other hand, earth-abundant thin film compounds have attracted substantial research interest towards developing commercially feasible low-cost and high-efficiency photovoltaic devices [3, 4]. For chalcopyrite structures, substituting In/Ga with Zn and Sn, which forms in the kesterite structure, are the most popular methods to reach a potential alternative material for a light-absorbing layer in thin film solar cell devices to replace conventional absorber layers [3, 4]. Considering the well-known CIS chalcopyrite thin film structure, a novel compound of the chalcopyrite type has been recently reported by replacing In with Zn [5, 6]. Starting from the initial attempts with Cu doping to the ZnSe structure, fabrication of Cu–Zn–Se ternary alloy became a point of interest as a cost-effective alternative to CIS in photovoltaic applications. In the literature, there are very limited works on this structure, and efforts are concentrated on the magnetically doped structure in ferromagnetic characteristics [5, 6]. Additionally, the works were aimed to use 2% doped CZSe thin film as an alternative absorber layer and the results on the application of dye sensitized solar cell were reported comparing with the undoped layer.

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In this work, Cu–Zn–Se (CZSe) compound was analyzed to determine their promising applications in the electronics and optoelectronic devices industries. Therefore, temperature-dependent current–voltage (I-V) characteristics of Ag/n-Si/p-CZSe/In were analyzed within the thermionic emission (TE) model to calculate the diode parameters and it was modified by the assumption of a Gaussian distribution (GD) of the barrier height. Moreover, to investigate interface states, capacitance–voltage (C-V) and conductance–voltage (G/w-V) characteristics were analyzed.

## 2. Experimental details

In this study, Cu–Zn–Se thin films were deposited by DC/RF magnetron sputtering technique on soda lime glass substrate (SLG) and (100) crystal oriented n-type Si wafer having the resistivity value of 1–10 Ωcm. CZSe thin film was obtained by sequential sputtering of Cu (99.999%), Se (99.999%), and ZnSe (99.99%) targets in the layer order of Se/ZnSe/Cu/ZnSe/Se/Cu/ZnSe/Se. In the sequentially stacked layer formation steps, the layer deposition order was chosen to eliminate the metallic film surface due to Cu aggregation. The thickness of these layers was optimized as 10, 50, and 60 nm, with the deposition rates at about 0.2, 1.0, and 2.0 Å/s for Cu, ZnSe, and Se layer deposition steps, respectively. During the deposition, the substrate temperature was kept constant at around 200 °C and base pressure of the sputtering system was $5 \times 10^{-6}$ Torr. Total thickness was measured as about 350 nm by Vecoo Dektak 6M thickness profilometer after the deposition. To investigate device characteristics, the back side of as-deposited n-Si substrate was coated with Ag metal contact using thermal evaporation technique and then, to enhance the ohmicity of the contacts, post-annealing treatment was done at 200 °C under the nitrogen atmosphere. In addition 200 nm thick In front contact layer was deposited onto the CZSe film surface through a shadow mask in circular dot contact shape of 2 mm diameter by using thermal evaporation method. Following this deposition process, the complete diode structure was annealed at 100 °C to enhance the quality of ohmic behavior of the contacts. The surface morphology and elemental composition of as-deposited films were determined by Quanta 400F field emission scanning electron microscope (SEM) equipped with energy dispersive X-ray spectroscopy (EDS) detector. Crystalline behavior of the films was investigated by Rigaku Miniflex X-ray diffraction (XRD) system equipped with CuKα X-ray source (λ = 1.54 Å). The optical measurement was performed by Perkin-Elmer Lambda 45 spectrophotometer. Van der Pauw configuration were used for electrical measurements and temperature-dependent conductivity measurements were done by using a Janish liquid nitrogen cryostat and Lake-Shore 331 temperature controller in the temperature interval of 80–450 K. In the Hall effect measurement, the current was applied by Keithley 220 current source and the voltage values were read from Keithley 619 electometer–multimeter. Walker Magnion Model FFD-4D electromagnet was used to produce a magnetic field in which the applied magnetic field strength was kept stable at around 0.90 T. Ag/n-Si/p-CZSe/In hetero-structure was analyzed by temperature-dependent I-V and room temperature C-V and G/w-V measurements. Keithley 2401 source-measure unit was used and the substrate temperature was varied from 220 to 360 K with the help of CTI-Cryogenics Model 22 refrigerator system combined with Model SC helium compressor. The frequency-dependent and G/w-V measurements at room temperature were also performed with the computer-controlled system by using Hewlett Packard 4192A LF model impedance analyzer.

## 3. Results and discussion

The CZSe thin films deposited on SLG substrates were used to investigate the material properties of this layer. From EDS analysis of the deposited film, the atomic percentage ratios were found as 12.9%, 18.3%, and 68.8% for Cu, Zn, and Se, respectively, where this result indicates the Se rich behavior of the deposited layer. From SEM microphotographs, the surface of the film was observed as smooth, compact, and densely packed morphology (Fig. 1). According to the XRD measurements (Fig. 2), the high intense reflection was observed at about $2\theta \sim 27.5°$ corresponding to the preferred orientation along the (112) direction, which belongs to ternary Cu III–VI systems [6]. Using transmittance spectrum of the film deposited on SLG substrate (Fig. 3*a*), the absorption coefficient was calculated as to be around $10^4$ cm$^{-1}$ and the direct band gap value for the film was determined as around 2.65 eV. In the electrical characterization step, the conductivity type of CZSe thin film structure was determined as p-type by calculation of Hall coefficient and this result was verified by the hot probe technique. Additionally, from Hall effect measurement, Hall mobility and hole concentration were found as about $2.4 \times 10^{14}$ cm$^{-3}$ and 3.5 cm$^2$/Vs, respectively. Temperature-dependent conductivity values were observed as having increasing behavior with increase in sample temperature and also illumination intensity

**Fig. 1.** SEM image of CZSe thin film layer.


**Fig. 2.** XRD pattern of CZSe thin film layer.

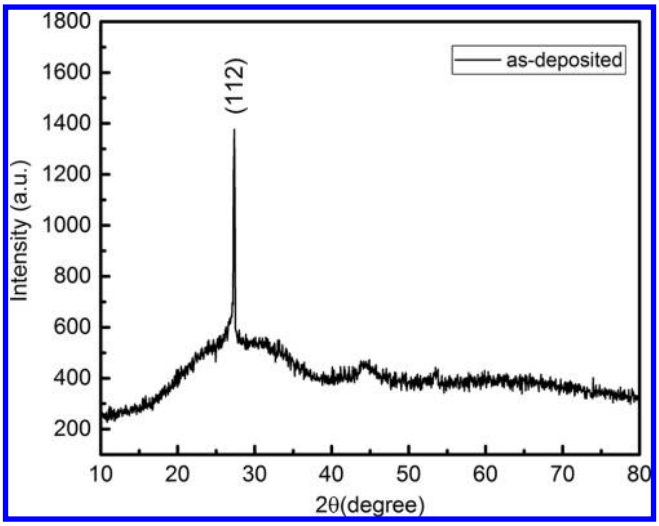


**Fig. 3.** (*a*) Transmittance spectrum (Inset shows the Tauc plot for band gap calculation) of CZSe thin film layer. (*b*) Temperature-dependent dark and illuminated conductivity behavior of CZSe thin film layer. [Colour online.]

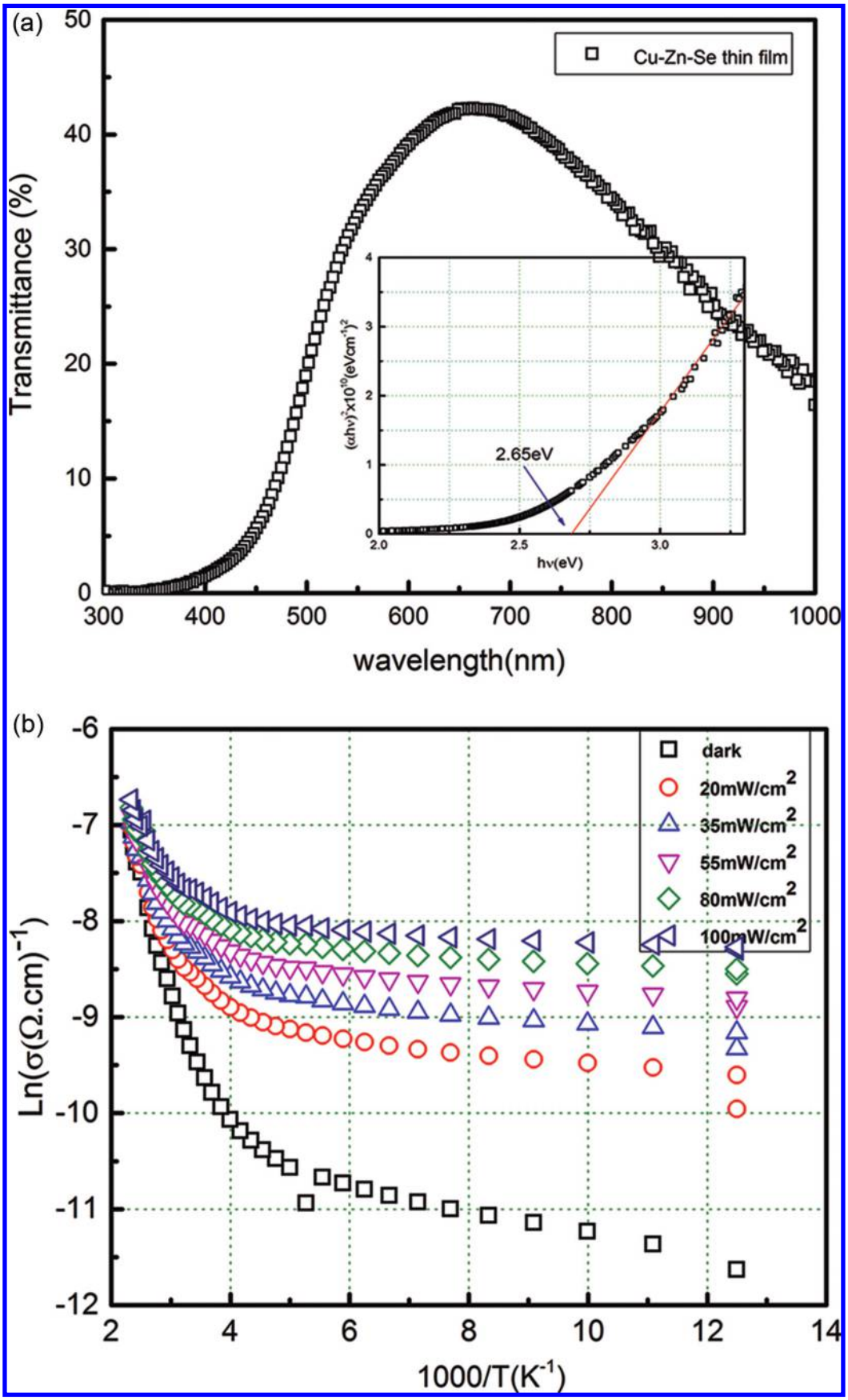
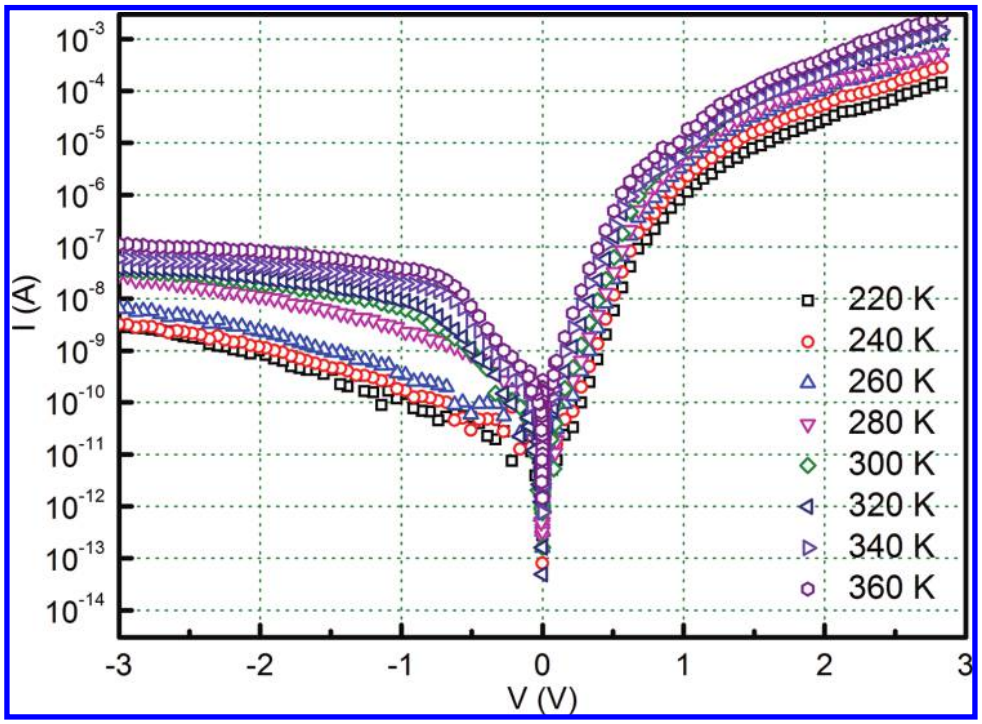


**Fig. 4.** The semi-logarithmic temperature-dependent forward and reverse bias I-V behavior of n-Si/p-CZSe diode. [Colour online.]




(Fig. 3*b*). The temperature-dependent dark-conductivity behavior showed Arrhenius behavior and it was modelled by TE theory with 192 and 65 meV activation energies in the high and low temperature regions, respectively.

I-V characteristics of Ag/n-Si/p-CZSe/In hetero-junction diode was investigated in the temperature interval of 220–360 K and the corresponding semi-logarithmic forward and reverse bias I-V behavior is presented in Fig. 4. Based on the TE model, the expression for the ideal current through a diode at a forward bias region is given as [7, 8]

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (1)$$

where the terms $I_0$, $q$, $V$, $k$, and $T$ are the reverse saturation current, electron charge, applied forward bias voltage across the junction, Boltzmann constant, and the ambient temperature, respectively. According to the TE theory, unity ideality factor ($n = 1$) corresponds to the ideal case; on the other hand, a deviation from pure TE model is usually observed in which $n > 1$ indicates the contribution of the other conduction mechanisms to the carrier transport in the junction region. Equation (1) was applied in the case of $V > 3kT/q$ to neglect the reverse current contribution [8]. In the general case, the applied bias voltage is shared by diode and series resistance $R_S$. However, the range in semi-logarithmic I-V data are in linear behavior, the voltage drop across $R_S$ can be assumed negligible in the analysis of the diode parameters [7]. $R_S$ is related to the resistance effects of both diode structure and contact regions that can play a role in current flow in the diode, therefore power and speed of the diode. At high forward voltage region, a deviation from the relation given in (1) was observed due to the series resistance effect, and for each diode temperature step, the value of this resistance was calculated from the parasitic resistance relation, $R_p = \partial V/\partial I$. As listed in Table 1, these values' decreases with increasing temperature may be due to the increase of $n$ and lack of free charge carriers at low $T$ region [8]. Thus, TE mechanism was applied to the experimental I-V data to extract the main diode parameters of the fabricated diode structure with respect to the change in ambient temperature. In (1), the term $I_0$ is related to the diffusive flow of minority carriers and the experimental $I_0$ values in terms of diode temperature can be derived from the straight line intercept of logarithmic forward bias current at zero bias point [7, 9]. These values were obtained from Fig. 4 for each temperature and listed in Table 1. From the $I_0$ relation given as;

**Table 1.** Diode parameters calculated for n-Si/CZSe diode.

| $T$ (K) | $n$ | $\Phi_{B0}$ (eV) | $R_S$ (kΩ) | $D_{it}$ (eV$^{-1}$cm$^{-2}$) |
|---|---|---|---|---|
| 220 | 3.91 | 0.560 | 29.778 | $3.272\times10^{13}$ |
| 240 | 3.26 | 0.692 | 27.135 | $2.661\times10^{13}$ |
| 260 | 2.65 | 0.790 | 22.548 | $2.474\times10^{13}$ |
| 280 | 2.46 | 0.890 | 20.990 | $1.856\times10^{13}$ |
| 300 | 2.28 | 0.960 | 19.379 | $1.593\times10^{13}$ |
| 320 | 2.03 | 0.999 | 12.844 | $1.353\times10^{13}$ |
| 340 | 1.92 | 1.100 | 8.407 | $7.878\times10^{12}$ |
| 360 | 1.81 | 1.200 | 5.890 | $6.296\times10^{12}$ |

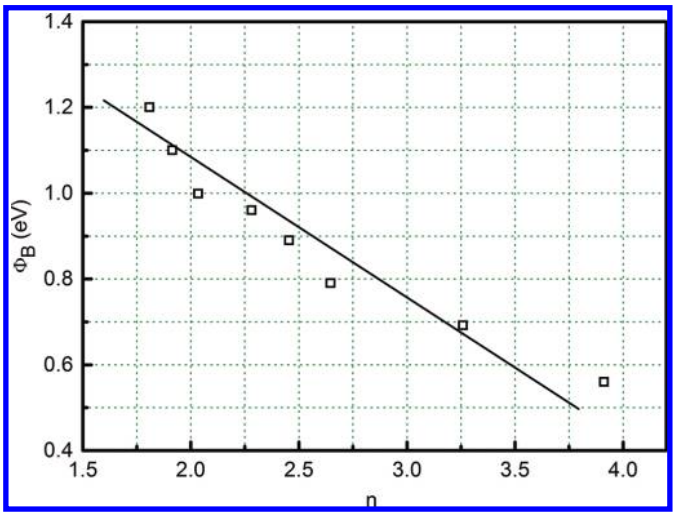
$$I_0 = AA^*T^2\exp\left(\frac{-q\Phi_{B0}}{kT}\right) \quad (2)$$

zero-bias barrier height $\Phi_{B0}$ can be obtained as a function of temperature with known diode area $A$ and the assumption on the effective Richardson constant $A^*$ [7]. The values of $n$ can also be determined by using (1) and semi-logarithmic plot of I-V, it can be expressed as [8]

$$n = \frac{q}{kT}\left[\frac{dV}{d\ln(I)}\right] \quad (3)$$

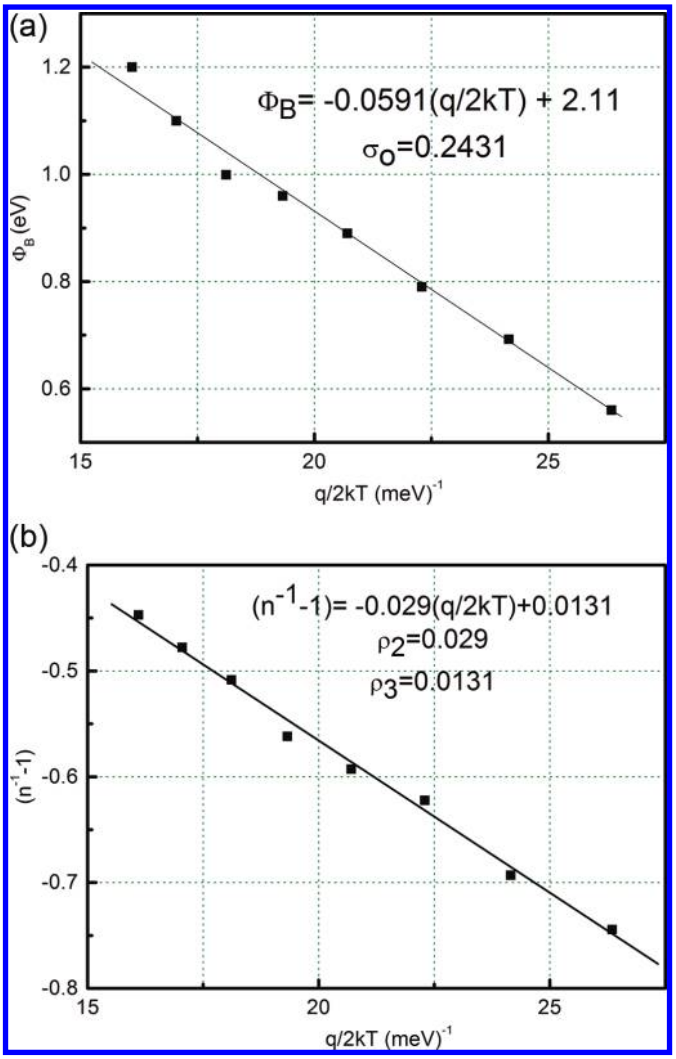
According to (3), $n$ values were calculated from the slope of the linear forward I-V curve represented in Fig. 4. The experimental

**Fig. 5.** Relation between $\Phi_{B0}$ and $n$ values for n-Si/p-CZSe diode. [Colour online.]




values of $\Phi_{B0}$ and $n$ obtained with assuming the validity of TE in the current flow were tabulated in Table 1. Both of these values were found to be strongly temperature dependent. As given in Table 1, the values of $\Phi_{B0}$ have increasing characteristics with increase in $T$ as different than the expected I-V behavior. When $T$ increases, carriers gain sufficient energy to overcome the potential barrier and contribute to the total current. On the other hand, at low temperature conditions, barrier inhomogenities with lower barrier patches affect the current flow, and the charge carriers can pass over the patches with lower barrier heights in the barrier formation in the diode [6–13]. The obtained $n$ values are in the range of 1.8–3.9 and they show a decreasing behavior with increase in $T$ as listed in Table 1. In addition to the fact that the current transport mechanism in the diode structure is contrary to TE and the additional mechanism can be required to explain the current flow through the junction, the high value of $n$ can be attributed to the native insulator layer formation at the junction interface and particular distribution of interface states localized in this region [14, 15]. The obtained $n$ and $\Phi_{B0}$ values are found to have a linear correlation and this behavior was shown in Fig. 5. According to Tung's approach, the observed linear behavior can be attributed to the lateral inhomogeneity of the barrier heights [13, 16] and it was analyzed by the linear fitting process. The extrapolation of the $\Phi_{B0}$ values to $n = 1$ in this plot gave the value of 1.23 eV, which is different from the band gap value of n-Si, and this result indicates that TE model cannot be the only predominant current transport mechanism in the diode. Based on the characteristics of the diode with calculated main diode parameters as a function of temperature, abnormal deviation in the fabricated diode from classical TE theory can be modelled by GD of the barrier height at the junction interface [12–14]. This model is applied under the assumption of barrier inhomogeneity with localized low barrier patches at the interface. In this case, current transport theories for homogeneous barrier height are extended to cover the effect of inhomogeneous barrier formation and the distribution of the inhomogeneity in the barrier height is explained with standard statistical distribution. The standard deviation $\sigma_0$ of this distribution roughly estimates the level of barrier inhomogeneities with respect to the mean value of barrier height $\overline{\Phi}_{B0}$ [13]. Therefore, with modification in barrier height, total current $I(V)$ through a barrier at forward bias region can be expressed as [12–14]

**Fig. 6.** (*a*) Plot of barrier height versus $q/2kT$ for n-Si/p-CZSe diode. (*b*) Plot of $n^{-1} - 1$ versus $q/2kT$ for n-Si/p-CZSe diode. [Colour online.]




$$I = AA^*T^2 \exp\left[\left(-\frac{qV}{kT}\right)\left(\overline{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT}\right)\right] \exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \quad (4)$$

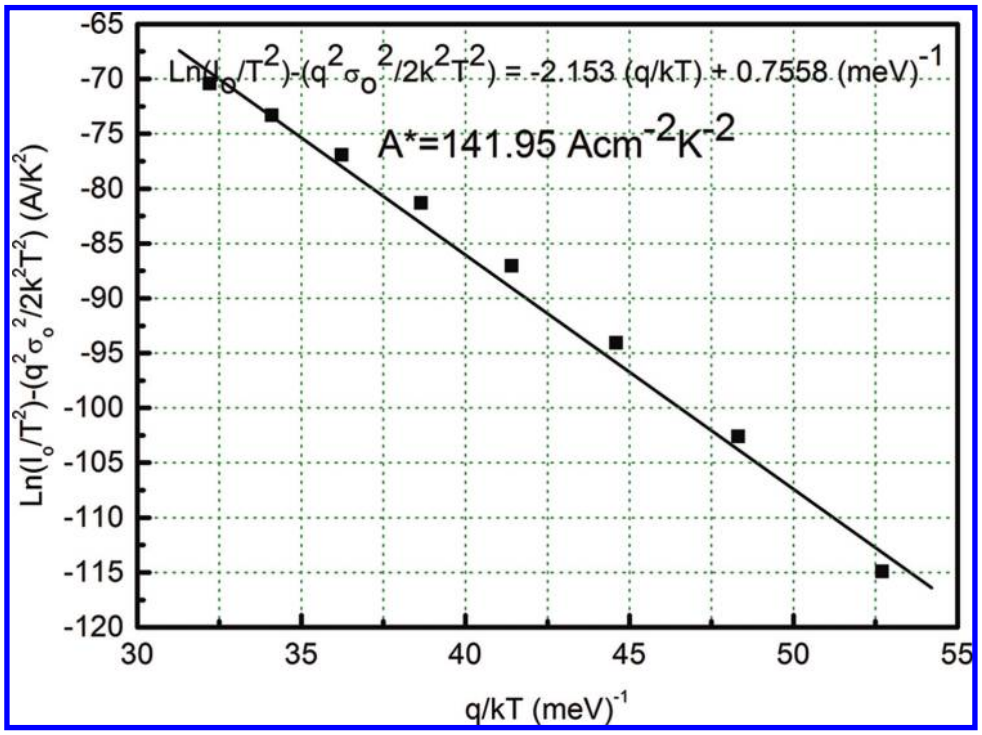
with modified reverse saturation current expression as,

$$I_0 = AA^*T^2 \exp\left(-\frac{q\Phi_{ap}}{kT}\right) \quad (5)$$

where $\Phi_{ap}$ and $n_{ap}$ are the apparent barrier height and ideality factor, respectively. In this expression, $\sigma_0$ gives the standard deviation in temperature dependence of barrier height and it is used to measure the deviation from the homogeneity of barrier height in the junction. From (4), the temperature variation of zero bias barrier height distribution can be represented in terms of GD as [14, 17],

$$\Phi_{ap} = \overline{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT} \quad (6)$$

**Fig. 7.** Plot of $\ln(I_0/T^2) - (q^2\sigma_0^2/2k^2T^2)$ versus $q/kT$ for n-Si/p-CZSe diode. [Colour online.]




As in the case of (6) there should be a linear relation between $\Phi_{B0}$ and $q/2kT$ (Fig. 6*a*) and from the straight line intercept and slope, $\overline{\Phi}_{B0}$ and $\sigma_0$ were calculated. Thus, $\sigma_0$ was obtained as 0.24 eV, which is about 12% of the mean value of barrier height, 2.11 eV. This result indicates the interfacial inhomogeneities with a GD of barrier heights at the interface [14]. The single straight line observed in Fig. 6*a* also verifies the presence of a single GD of barrier height. In this model, the variation of $n_{ap}$ with $T$ is given by [14, 17]

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{7}$$

where $\rho_2$ and $\rho_3$ are the parameters related to voltage deformation of the barrier height distribution. In this case, $\sigma_0$ and $\overline{\Phi}_{B0}$ are linearly bias dependent with $\rho_2$ and $\rho_3$, respectively. As shown in Fig. 6*b*, linear behavior of the plot of $(n^{-1} - 1)$ versus $q/2kT$ confirms voltage deformation of the GD of the barrier height in terms of calculated $n$ values [10, 11] and by applying linear fitting process to the straight line in this plot, the voltage coefficients were calculated from the slope and intercept as, $\rho_2 = 0.029$ V and $\rho_3 = 0.013$, respectively. With the observation of barrier inhomogeneity, according to GD of the barrier heights, the modified Richardson equation can be expressed as [14]

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_0^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\overline{\Phi}_{b0}}{kT} \tag{8}$$

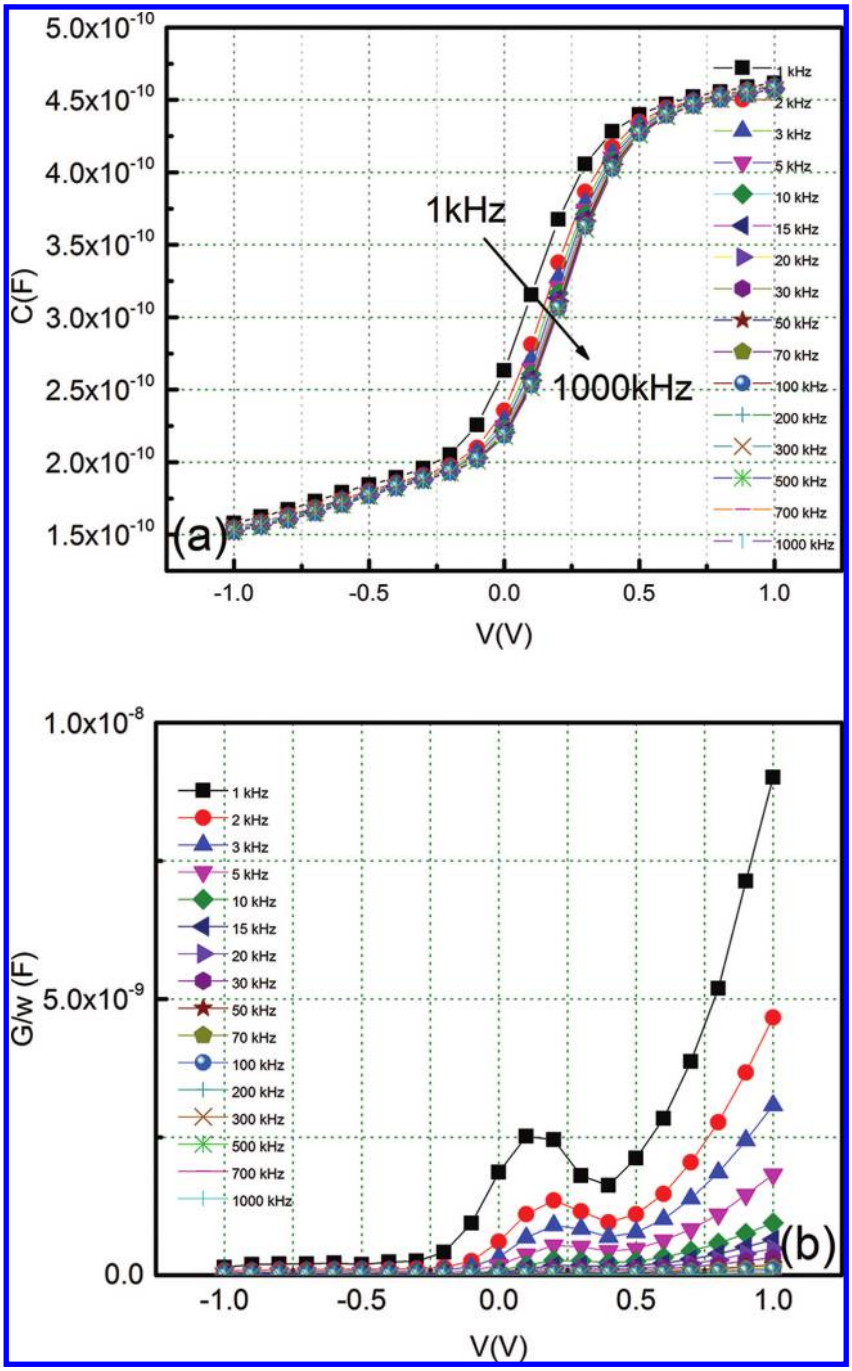
From this relation, the Richardson plot $\ln(I_0/T^2)$ versus $1/T$ was modified as $\ln(I_0/T^2) - (q^2\sigma_0^2/2k^2T^2)$ versus $q/kT$ given in Fig. 7. Using the experimental $I_0$ values, $\overline{\Phi}_{b0}$ and modified Richardson constant $A^*$ were obtained with the slope and the intercept of the straight line as 2.15 eV and 141.95 $Acm^{-2}K^{-2}$, respectively.

C-V and G/w-V measurements in the frequency range of 1–1000 kHz at room temperature were carried out to investigate interface states of n-Si/p-CZSe hetero-structure (Fig. 8). As shown in Fig. 8*a*, the capacitance ($C$) values are observed as having slight decreasing behavior with increase in the applied frequency. On the other hand, as indicated in Fig. 8*b*, there is a strong dependence on the conductance ($G/w$) values with the frequency, and a distinctive peak at depletion region for each frequency was observed due to the particular distribution of density of interface states ($D_{it}$) at the junction of n-Si/p-CZSe structure [18]. Moreover, the high values of $C$ and $G/w$ at low frequency can be attributed to the presence of interface states that can easily follow an AC signal and this can result in excess capacitance and conductance. On the other hand, interface states cannot follow the AC signal at high frequency [19]. From the results of the C-V measurements, high–low frequency capacitance ($C_{HF}$–$C_{LF}$) and Hill–Coleman methods were applied to determine interface state density ($D_{it}$) [18, 20, 21]. $C_{HF}$–$C_{LF}$ method is the most suitable technique to achieve $D_{it}$–$V$ profile in which the interfacial layer capacitance ($C_i$) is assumed to be connected in series to the parallel combination of interface state capacitance ($C_{ss}$) and the space charge capacitance ($C_{sc}$) [22]. Therefore, $D_{it}$ is calculated at given bias as follows:

$$qAD_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1} \tag{9}$$

where the parameters $q$, $A$, $C_{HF}$, and $C_{LF}$ are the elementary charge, active diode area, the highest frequency capacitance (1 MHz) and the lowest frequency capacitance (1 kHz), respectively. As a result of this analysis, the variation of $D_{it}$ with respect to applied bias voltage obtained from $C_{HF}$–$C_{LF}$ method is presented in Fig. 9*a*. To get more detailed information about interface state density distribution, Hill–Coleman method was carried out using the following equation [21]:

**Fig. 8.** (*a*) C-V characteristics of n-Si/p-CZSe diode. (*b*) G/w-V characteristics of n-Si/p-CZSe diode. [Colour online.]



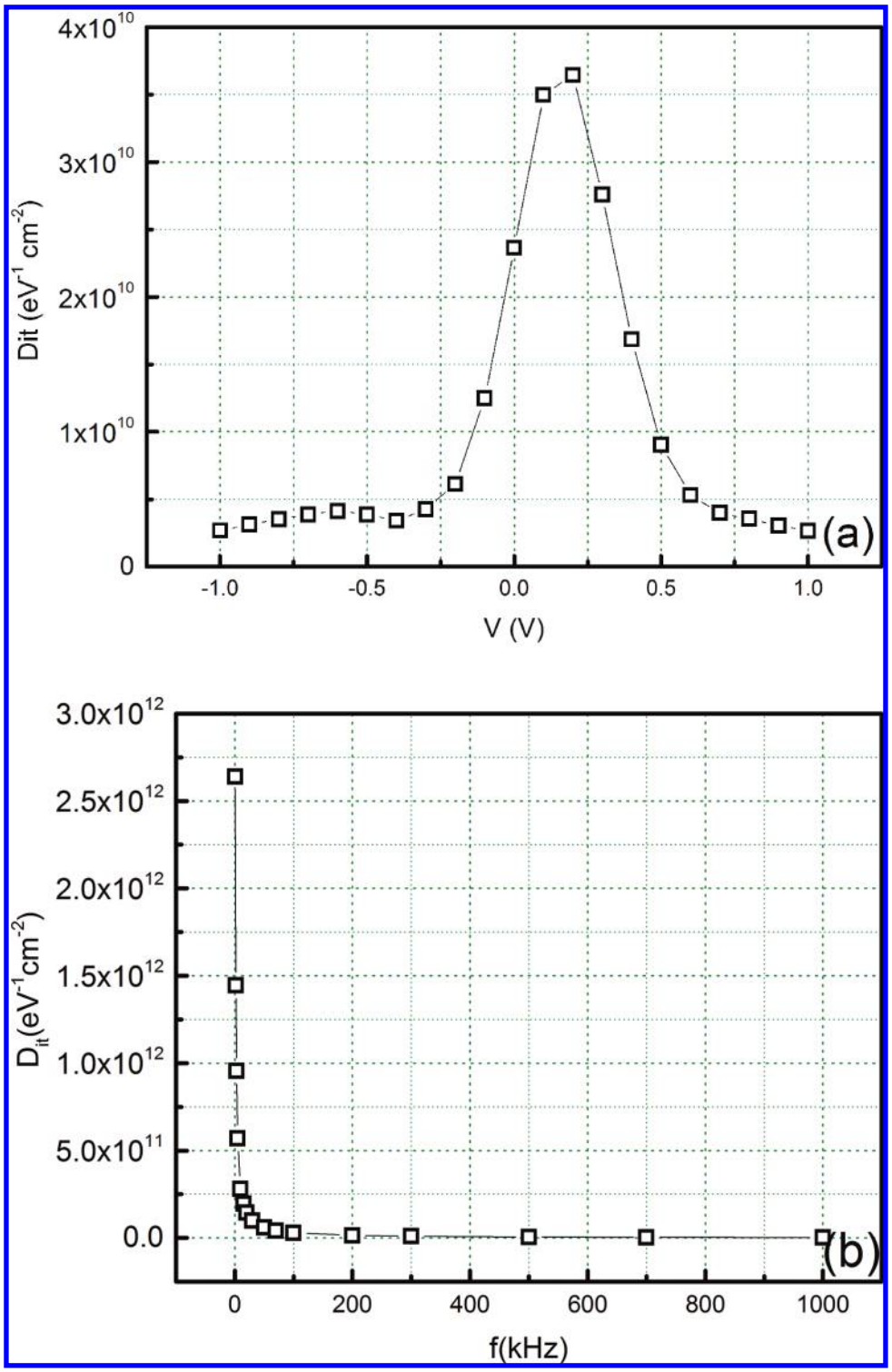

$$D_{it} = \left(\frac{2}{qA}\right)\frac{(G_m/w)_{max}}{[(G_m/w)_{max}/C_i]^2 + (1 - C_m/C_i)^2} \quad (10)$$

where $w$ is angular frequency, and $C_m$ and $(G_m/w)_m$ are the measured capacitance and conductance, respectively, corresponding to peak value. The frequency-dependent interface state distribution was given in Fig. 9*b* and it is clearly observed that there is an exponential decrease with increasing frequency associated with the inability of interface states to follow AC signal at high frequency. In addition, the non-ideal current behavior deviation from the ideal case was attributed to the saturation effects due to dominant effects of $D_{it}$ and $R_S$ at the high forward bias region. Therefore, $D_{it}$ values can also be calculated using the results of the forward bias I-V measurements by considering the interface states in equilibrium with the semiconductor. With the values of $n$ greater than unity, $D_{it}(V)$ can be expressed as [23]

$$D_{it}(V) = \frac{1}{q}\left\{\frac{\varepsilon_i}{\delta}[n(V) - 1] - \frac{\varepsilon_s}{W_D}\right\} \quad (11)$$

where $W_D$ is width of the depletion region, $\delta$ is the thickness of interfacial layer, and $\varepsilon_s$ and $\varepsilon_i$ are the permittivity of semiconduc-

**Fig. 9.** (*a*) Interface state density profile obtained from $C_{HF}$–$C_{LF}$ method. (*b*) Interface state density profile obtained from Hill-Coleman method. [Colour online.]




tor and interfacial layer, respectively. Using (11), $D_{it}$ was evaluated as a function of $E_C - E_{SS}$ for each temperature as given in Fig. 10. The energy of interface states, $E_{SS}$, with respect to the top of the conduction band at the surface of the semiconductor is defined as

$$E_c - E_{ss} = q(\phi_e - V) \tag{12}$$

with the effective barrier height $\Phi_e$ being a voltage-dependent parameter with the possibility of an interface state in the diode structure [23, 24]. As a result of this analysis, the obtained $D_{it}$ values were observed in increasing behavior with the increasing temperature (Fig. 10). In further analysis on the fabricated diode structure, it is important to determine $R_S$ values in addition to $D_{it}$.

**Fig. 10.** Graph of density of interface states as a function of ($E_C - E_{SS}$) obtained from the temperature-dependent I-V measurements. (The inset shows the variation of density of interface states with respect to temperature). [Colour online.]

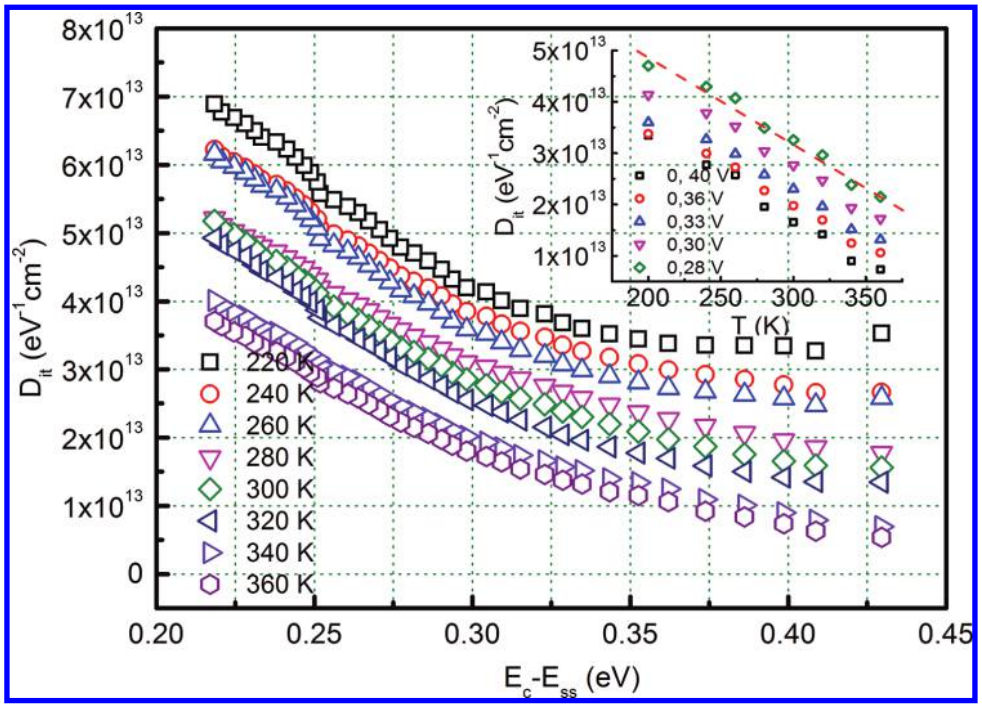
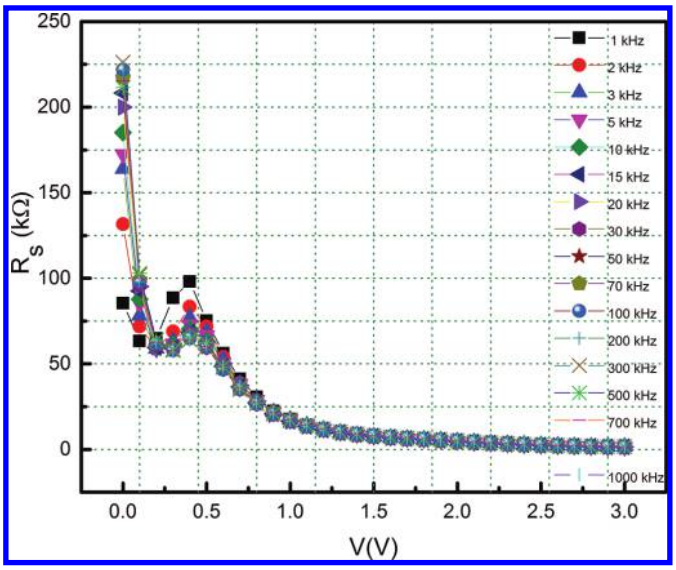



**Fig. 11.** The graph of series resistance values as a function of applied voltage and frequency. [Colour online.]




To evaluate these values, the admittance method developed by Nicollian and Brews was applied to the experimental data. In this technique, voltage-dependent $R_S$ can be obtained using the following expression [13]:

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \quad (13)$$

where $G_{ma}$ and $C_{ma}$ are the measured conductance and capacitance, respectively, in the strong accumulation region. Figure 11 shows the variation of $R_S$ with the applied bias voltage in the frequency range of 1 kHz – 1 MHz. From the plot of $R_S$ as a function of voltage, the values of $R_S$ were found to be strongly dependent on frequency and applied bias voltage. In addition, an anomalous peak was observed in between 0.1 and 0.5 V, and the magnitude of the peak decreases as the frequency increases. This result can be attributed to reordering or restricting under the applied voltage [25].

## 4. Conclusion

In this present work, CZSe semiconducting thin film structure was investigated for possible device applications. According to the TE model, the main diode parameters were calculated and the diode was found in non-ideal behavior with high values of ideality factor. The current behavior was assumed to be dependent especially on interfacial layer, interfaces states, and series resistance and then modeled by the anomaly in TE method. The modification of total current flow by assuming GD of the barrier height, where the mean value of barrier height was 2.11 eV with standard deviation of 0.24 eV. Moreover, the value of the modified Richardson constant was determined as 141.95 $Acm^{-2}K^{-2}$, consistent with the literature. From the frequency-dependent C-V and G/w-V measurements, the formation of the interfacial states was investigated under the assumption of native insulator layer at the junction interface. As a result of the calculations with high–low frequency capacitance ($C_{HF}$–$C_{LF}$) and Hill–Coleman methods, $D_{it}$ values were found to have increasing behavior with increases in frequency. Furthermore, $R_S$ values were found to be strongly dependent on frequency and applied bias voltage.

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