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Analysis of current conduction mechanism in CZTSSe/n-Si structure

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Abstract

In this study, $Cu_2ZnSn(S,Se)_4$ (CZTSSe) thin films were deposited by the single step thermal evaporation process using the sintered powder of CZTSSe on soda lime glass (SLG) and Si wafer substrates. The structural, optical, and electrical properties of deposited films were investigated. Current–voltage (I–V) in the temperature range of 250–350 K, capacitance–voltage(C–V) and conductance–voltage (G/w–V) measurements at room temperature were carried out to determine electrical properties of CZTSSe/n-Si structure. The forward bias I–V analysis based on thermionic emission (TE) showed barrier height inhomogeneity at the interface and thus, the conduction mechanism was modeled under the assumption of Gaussian distribution of barrier height. The mean barrier height ($\bar{\Phi}_{B0}$) and standard deviation (σ_0) at zero bias were obtained as 1.27 eV and 0.18 V, respectively. Moreover, Richardson constant was obtained as 120.46 A cm^{-2} K^{-2} via modified Richardson plot and the density of interface states (D_{it}) profile was determined using the data obtained from forward bias I–V measurements. In addition, by the results of frequency dependent C–V measurements, characteristics of the interface state density were calculated applying high-low frequency capacitance ($C_{HF} - C_{LF}$) and Hill–Coleman methods.

1 Introduction

In recent years, $Cu_2ZnSn(S,Se)_4$ (CZTSSe) thin films have been of great interest in the photovoltaic technology as an absorber layer due to the convenient optical properties. They have high absorption coefficient in the order of 10^4 cm^{-1} and the direct band gap energy that can be tuned between 1.0 and 1.5 eV [1–3]. Furthermore, these quaternary compounds including Cu_2ZnSnS_4 (CZTS) and $Cu_2ZnSnSe_4$ (CZTSe) called as kesterites are considered to be an attractive alternative compound semiconductors to chalcopyrite CIGS since they consist of non-toxic, earth-abundant and low-cost elements [4, 5]. There have been several scientific works in the literature for the deposition of kesterite thin films by using the vacuum and non-vacuum growth techniques like thermal evaporation [6], magnetron sputtering [7], spray pyrolysis [8] and sol–gel [9] methods. The best power conversion efficiencies have been reported as 8.4 and 9.15% for CZTS and CZTSe thin films based solar cells, respectively [6, 10]. Moreover, 12.6% efficient solar cell based on CZTSSe thin film has been achieved by using hydrazine-based solution deposition process which pave the way for future prospects [11]. In addition, post-selenization is prevalent method for fabrication of CZTSe and CZTSSe films that requires high substrate temperature [12–14].

In this study, the focus is mainly on producing CZTSSe thin films with an efficient and cost-effective way by excluding any other auxiliary/additional deposition steps like selenization and sulphurisation processes while maintaining the high quality in terms of physical properties of the films. The CZTSSe/n-Si heterojunction device fabrication was also studied in order to reach the high device performance parameters for possible future applications in various technologies. In this manner, the CZTSSe thin films were deposited by a single-step thermal evaporation process on both soda-lime glass (SLG) and silicon substrates, in which the sintered $Cu_2ZnSn(S,Se)_4$ powder was used as an evaporation

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source. Furthermore, the structural, optical and electrical characterization of the thin films on SLG substrates were investigated. On the other hand, the detailed information about the electronic properties of the fabricated CZTSSe/n-Si heterojunction diode structure were determined by means of temperature dependent current–voltage (I–V) and capacitance–voltage (C–V) measurements. The total current flow in the junction was found under the effect of localized low potential patches, and therefore the origin of the barrier inhomogeneity was discussed by assuming a Gaussian distribution on the barrier height. In addition, the distribution of the interfacial states over the barrier height was investigated to explain the carrier transport characteristics in the diode. Although there are few studies on the device fabrication based on CZTSSe thin film/Si structure, to the best of our knowledge this work is the first attempt to realize conduction mechanism of the CZTSSe/Si heterostructure.

2 Experimental details

$Cu_2ZnSn(S,Se)_4$ source powder was produced by sintering process. For this process; Cu, Zn, Sn, S, and Se materials having 99.99% purity were inserted into a chemically cleaned quartz ampoule. Then, the ampoule was evacuated down to a vacuum level of around 10^{-5} Torr and sealed. The sealed quartz ampoule was placed into the vertical furnace for sintering process and steadily heated up to 1150 °C with a rate of 100 °C h^{-1} and kept at this temperature for 48 h. Subsequently, it was cooled down to room temperature slowly. After completing the sintering and subsequent cooling processes, the evaporation source was prepared in a powder form by using the pieces taken from the different part of the ingot. The elemental composition of powder was analyzed by energy dispersive X-ray spectroscopy (EDXA) and the atomic weight percentage of the constituent Cu, Zn, Sn, S, Se elements were determined as 22, 10, 13, 21, 34%, respectively. Then, CZTSSe thin films were deposited by thermal evaporation on soda-lime glass (SLG) substrates and n-type Si (100) wafers with the resistivity value of 1–10 Ω-cm. During the deposition, the substrate temperature was kept at room temperature; additionally, the crucible temperature was controlled in the range of 900–1100 °C to minimize the variation of the growth rate and keep stable at about 2–4 Å s^{-1} under vacuum of about 10^{-5} Torr. Before the deposition, the glass substrates were ultrasonically cleaned in acetone, isopropanol and H_2O_2:H_2O (1:3) for 10-min in each step. In order to remove natural oxide layers on the surfaces of the Si wafers, the etching treatment by HF:H_2O (1:10) solution was applied. The back surface Ag contact was performed by thermal evaporation and annealed at 350 °C under nitrogen (N_2) flow to provide the ohmic behavior of the contacts. Following to the deposition of the CZTSSe thin film, all samples were annealed at 350 °C under N_2 atmosphere to improve the CZTSSe structure. Subsequently, the front indium (In) ohmic contact was deposited to the film surface by using copper dot masks 700 µm in diameter to complete In/CZTSSe/n-Si/Ag sandwich structure.

The morphological and compositional properties of the deposited films and the layer characteristic in the heterostructure were investigated by Quanta 400 FEG model scanning electron microscopy (SEM) equipped with energy dispersive X-ray spectroscopy analysis (EDXA) system. The surface morphology of the thin films was studied by atomic force microscopy (AFM) technique using a Veeco Multimode V AFM system. The thicknesses of the as-grown and annealed films on SLG substrate were also measured electromechanically by a Dektak 6M profilometer. The X-ray diffraction (XRD) measurements were performed by using a Rigaku Miniflex XRD system equipped with CuKα radiation source having wavelength 1.54 Å. Raman scattering measurements were carried out by using a Horiba-Jobin Yvon iHR550 imaging spectrometer with a three-grating monochromator and a laser with the wavelength of 532 nm used as an excitation source. Spectral transmission and reflection measurements were recorded with Perkin-Elmer LAMBDA 45 UV/VIS/NIR spectrophotometer in the wavelength region of 300–1000 nm. Room temperature Hall effect measurement was also measured to determine the electrical properties of the films by using Nanomagnetic Hall Effect system at a magnetic field strength of 0.9 T. In order to investigate the device parameters of In/CZTSSe/n-Si structure, temperature dependent current–voltage (I–V) measurements without illumination were carried out using the computer-controlled measurement setup with a Keithley 2401 sourcemeter, Model 22 CTI Cryogenics closed-cycle helium cryostat and LakeShore DRC-91C temperature controller. In addition, HP 4192A LF Impedance Analyzer was used for the measurements of capacitance–voltage (C–V) and conductance–voltage (G–V) of the devices. A study of the photo-electrical measurements was carried out to determine the photovoltaic behaviors by using Newport solar simulator and basic parameters were calculated by performing forward bias I–V curve analysis under dark and illumination of 100 mW cm^{-2}.

3 Results and discussion

3.1 Material properties of the thin film layer

Elemental composition analysis of the deposited film was acquired from EDXA measurement. The atomic percentage ratios were determined as 8, 10, 24, 24, 34% for Cu, Zn, Sn, S, Se, respectively. It indicates that the deposited film has Cu poor, Sn rich compositions. Since the powder source was sintered from the constituent elements, it is expected to be

a single source (quaternary compound) that can be evaporated in a distinct evaporating temperature and a growth rate. However, CZTSSe bulk is the alloy of five elements Cu, Zn, Sn, Se, and S, the alloy can be decomposed into these elements or binary/ternary compound during the process of single-thermal evaporation, in which each material would have different melting point and different vapor pressure. In other words, under certain conditions, quaternary alloy source may decompose and physically at low temperatures, elements and/or decomposed compound structures with having high vapor pressure can start to evaporate independent from the bulk material. XRD patterns of the film is shown in Fig. 1. No entries about mixed, elemental S and Se phases have been observed except Sn(S,Se) secondary phases by ICDD XRD database search. It is expected that peak position of CZTSSe phases shifts towards the higher diffraction angle depending on the ratio of S/(S + Se) in XRD spectrum [15]. The main diffraction peak from (112) plane is detected at 2θ = 28.1°, which is attributed to the phase of CZTSSe compound (*ICDD data #00-052-0868 CZTSe and ICDD data#00-026-0575 CZTS*) [16]. Secondary phases labeled as Sn(S,Se) phases are also detected in XRD pattern of the film (*ICDD data#00-048-1224 SnSe and ICDD data#00-039-0354 SnS*). The one of the most probable reasons of the existence of secondary phases is the off-stoichiometric film composition. Raman measurement with 532 nm excitation wavelength was applied to obtain more detail information about the structural analysis and to determine the mixed and secondary phases in the film structure. Raman spectrum of the deposited film is given in Fig. 2. The vibration of the anion A_1 modes of CZTSe and CZTS compounds are observed in 196 and 338 cm^{-1} in Raman spectrum, respectively. On the other hand, in CZTSSe compound, there is

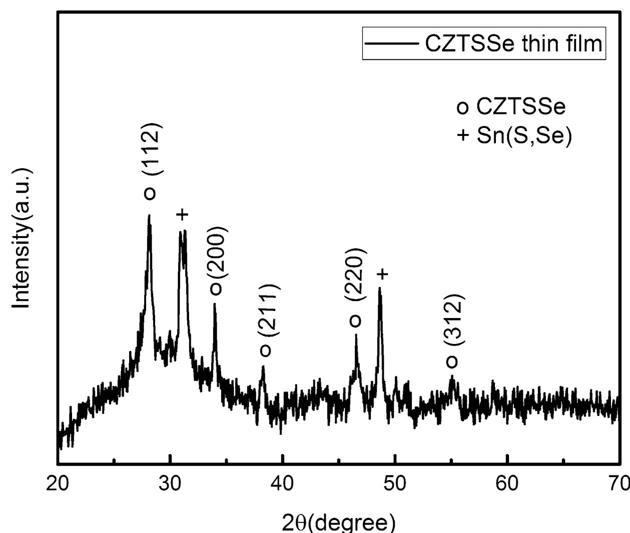

Fig. 1 XRD pattern of CZTSSe thin films

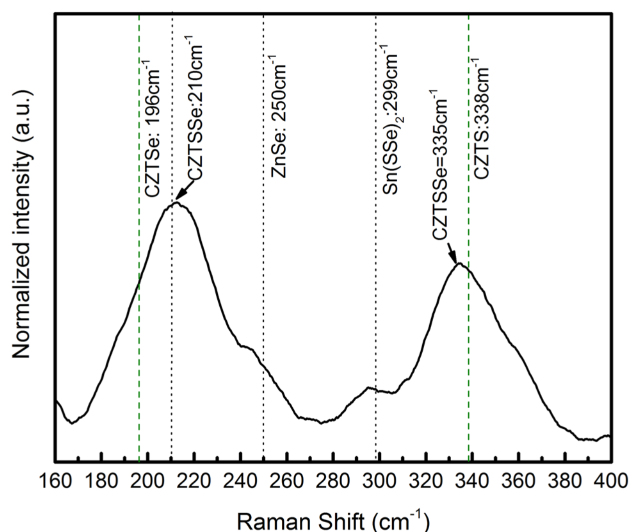

Fig. 2 Raman spectrum of CZTSSe film

bimodal behavior in Raman spectrum and shift of the A_1 modes is observed to the higher wavenumbers with increasing the ratio of S/(S + Se) [17]. The variation of A_1 modes is clearly presented in Fig. 2. The obtained spectrum was fitted using mixed of Gaussian and Lorentzian function to resolve the secondary peaks. Two peaks centered at 250 and 299 cm^{-1} were also observed corresponding to ZnSe and $Sn(S,Se)_2$, respectively [18, 19]. The broaden Raman peak indicates that there is a structural disorder due to the random distribution of S and Se atoms in the lattice, which gives rise to fluctuation in the masses and the force constants with the neighbors [17]. In order to get the information about the film surface morphology, the cross sectional and surface SEM micrographs of CZTSSe film and AFM images were obtained and they are given in Figs. 3 and 4, respectively. As seen from Fig. 3a, the thickness of film was determined from cross-sectional SEM image to be about 910 nm and this result is very close agreement within the measurement uncertainty with the value determined by Dektak 6M thickness profilometer measurement as about 900 nm. Figure 3b indicates the surface of film having compact and densely packed morphology. As seen from AFM images of deposited film in Fig. 4, the surface roughness of the film is around 44 nm which indicates the highly rough surface characteristics. Considering 2D AFM image, this rough surface is attributed to the large columnar structure related with the segregation of the constituent elements as observed from the SEM image.

Furthermore, spectral transmission and reflection measurements were carried out at room temperature by UV/Vis/NIR spectrometer. Transmission and absorption spectra for CZTSSe deposited on SLG are given in Fig. 5. The optical absorption coefficient was calculated from the spectral

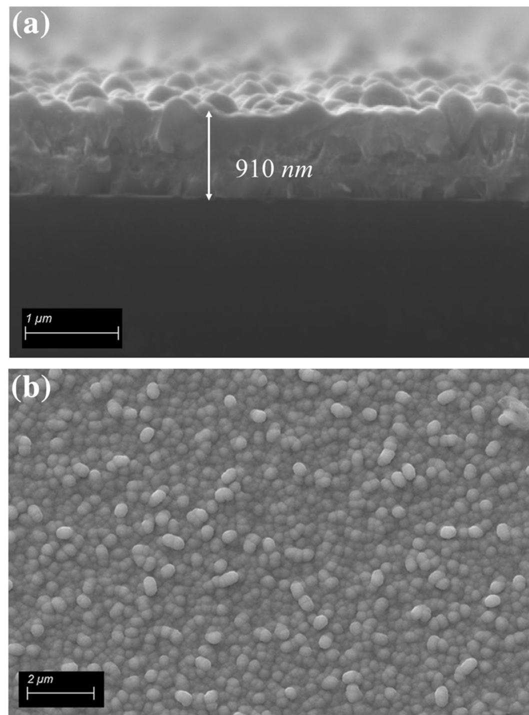

Fig. 3 SEM micrographs obtained from **a** the cross section and **b** the top view of CZTSSe thin film

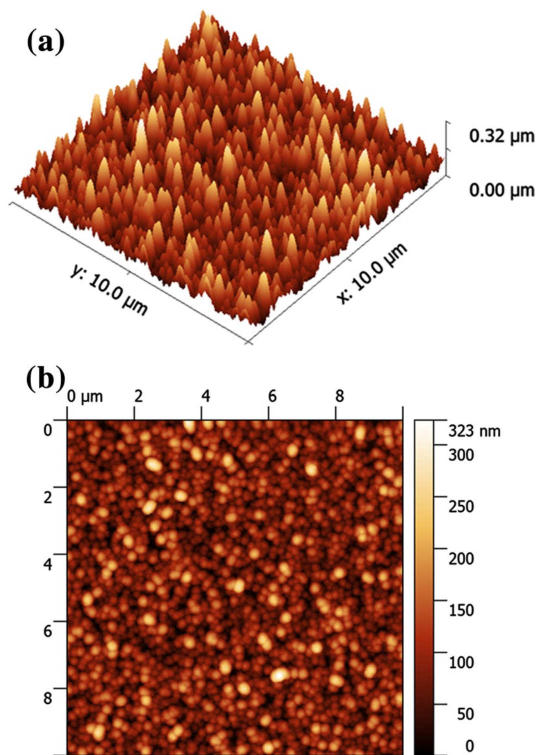

Fig. 4 3D and 2D AFM images of CZTSSe thin film

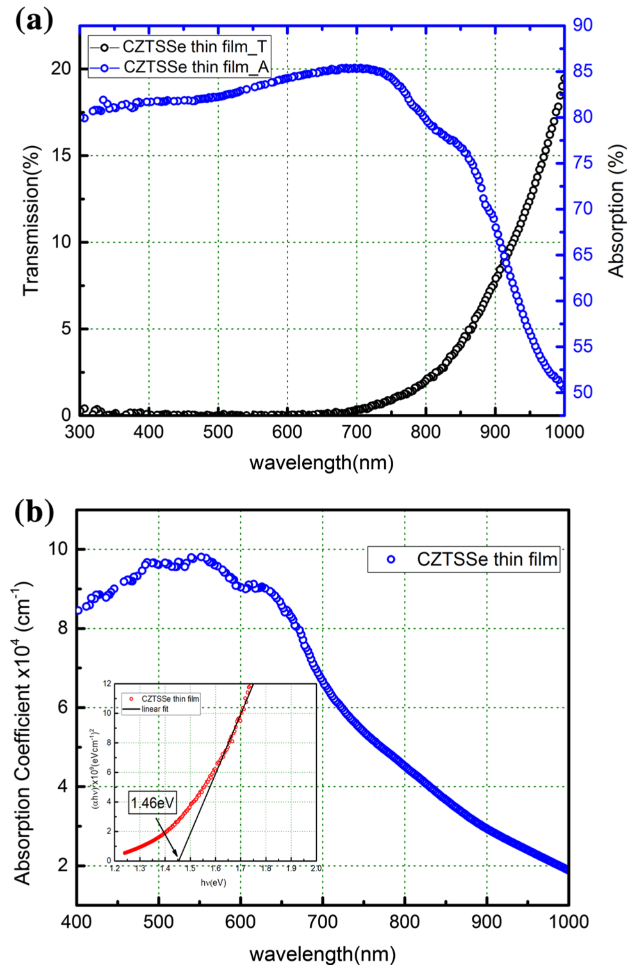

Fig. 5 Transmission and absorption spectra of CZTSSe film (**a**), absorption coefficient vs. wavelength graph (**b**) the inset shows $(\alpha h\nu)^2$ vs. $h\nu$ plot

measurements of transmittance (T) and reflectance (R) by using the equation [20],

$$T = (1 - R)^2 e^{-\alpha t} \quad (1)$$

where α is absorption coefficient, t is the thickness of the films. The values of α depending on the wavelength are given in Fig. 5b. As seen from the Figure, the absorption coefficient is above 10^4 cm^{-1}, and is in good agreement for the absorber materials reported in the literature [21]. Moreover, the optical band gap value was evaluated by using the expression [20],

$$(\alpha h\nu) = A(h\upsilon - E_g)^{1/2} \quad (2)$$

where A is constant, $h\nu$ is the incident photon energy, E_g is the optical band gap. The optical band gap was estimated by extrapolating the linear part of the plot to energy axis. As seen from inset of Fig. 5b, it was obtained as 1.46 eV. So, it is well-consistent with the reported band gap values

of CZTSe and CZTS structures lying in between 1.0 and 1.5 eV [2, 3].

In order to get the electrical properties of the film, resistivity and Hall Effect measurements on the samples having van der Pauw geometry were performed at room temperature. CZTSSe film showed p-type semiconductor behavior as observed from the sign of Hall voltage and Seebeck voltage. The average values of resistivity, carrier concentration and mobility of the samples were obtained as 2.84 Ω cm, 2.41×10^{17} cm^{-3} and 9.12 cm^2/V s, respectively.

3.2 Device properties

3.2.1 Current–voltage (I–V) measurement

The set of temperature dependent forward and reverse bias current–voltage (I–V) curves for CZTSSe/n-Si diode with effective diode area of 15×10^{-3} cm^2 is shown in Fig. 6. These measurements were used in order to investigate the main diode parameters and to determine the dominant conduction mechanisms through the junction. From Fig. 6, the reverse bias current values indicate a good saturation behavior while the forward current is observed in exponential increasing behavior with increasing of bias voltage. The rectifying characteristics of the junction were determined by calculating rectification factor (RF), which is the ratio of forward current to reverse current at constant bias voltage, and calculated as two orders of magnitude at room temperature. This ratio of the current was observed in increasing behavior with increase in bias voltage at each temperature and the decreasing behavior with increase in temperature at each bias voltage. This type of variation in RF values with temperature and bias voltage can be due to the effect of the trap levels localized at the interface and the inhomogeneous trap distribution in the bulk of heterostructure [22, 23]. Since thermionic emission (TE) is one of the most dominant carrier conduction mechanisms in the semiconductor diodes [24–27], initially it was adopted to the experimental I–V data to describe the current through the barrier potential in the diode. According to TE model, I–V relationship of junction of the diode can be described as [24, 25];

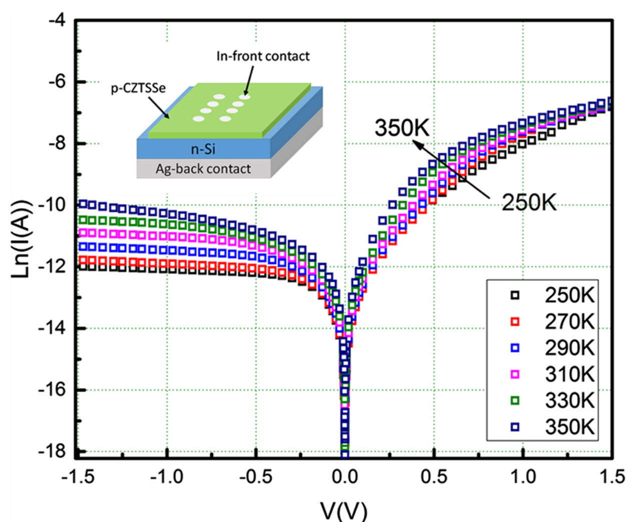

Fig. 6 Temperature dependent I–V curves of CZTSSe/n-Si diode. The inset shows schematic diagram of In/CZTSSe/n-Si/Ag heterojunction sandwich structure

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \tag{3}$$

where I_0 is the reverse-saturation current, q is the electronic charge, V is the applied forward bias voltage, k is the Boltzmann constant, n is the ideality factor and T is the absolute diode temperature. As shown in Fig. 6, the I–V curves in the semi-logarithmic scale deviates from linear behavior above the bias voltage of about 0.5 V. The deviation at high forward bias region can be observed due to the effect of series resistances (R_s) and interface states (N_{ss}) [24–30]. Therefore, using Eq. 3 in the case of $V > 3$ kT/q, main diode parameters can be extracted from TE theory without any reverse current contribution, [25] and series resistance effect can also be eliminated when working on this region of interest [31–33]. From Eq. 3, I_0 values were derived by extrapolating forward bias ln I–V plot (Fig. 6) and so that zero-bias barrier height (Φ_{B0}) was calculated from these values by using the relation;

$$I_0 = AA^*T^2\exp\left(\frac{-q\Phi_{B0}}{kT}\right) \tag{4}$$

where A is the effective area of the diode and A^* is the effective Richardson constant. By applying TE model, A^* value can be approximated to the typical value for n-type Si as 112 A cm^{-2} k^2 [28, 34] under the assumption of uniform barrier height formation in the diode. Experimental values of I_0 and Φ_{B0} for each temperature step are listed in Table 1. The temperature dependency of Φ_{B0} is also represented in Fig. 7a and the increase in Φ_{B0} with increasing temperature can be related to the improvement in CZTSSe film structure

Table 1 Diode parameters calculated by applying TE theory

Temperature (K)	Ideality factor(n)	Saturation current (I_o)	Barrier height (Φ_{B0})
250	4.82	1.17×10^{-6}	0.55
270	4.42	1.23×10^{-6}	0.58
290	4.10	1.25×10^{-6}	0.62
310	3.80	1.45×10^{-6}	0.66
330	3.29	1.63×10^{-6}	0.71
350	2.89	2.12×10^{-6}	0.75

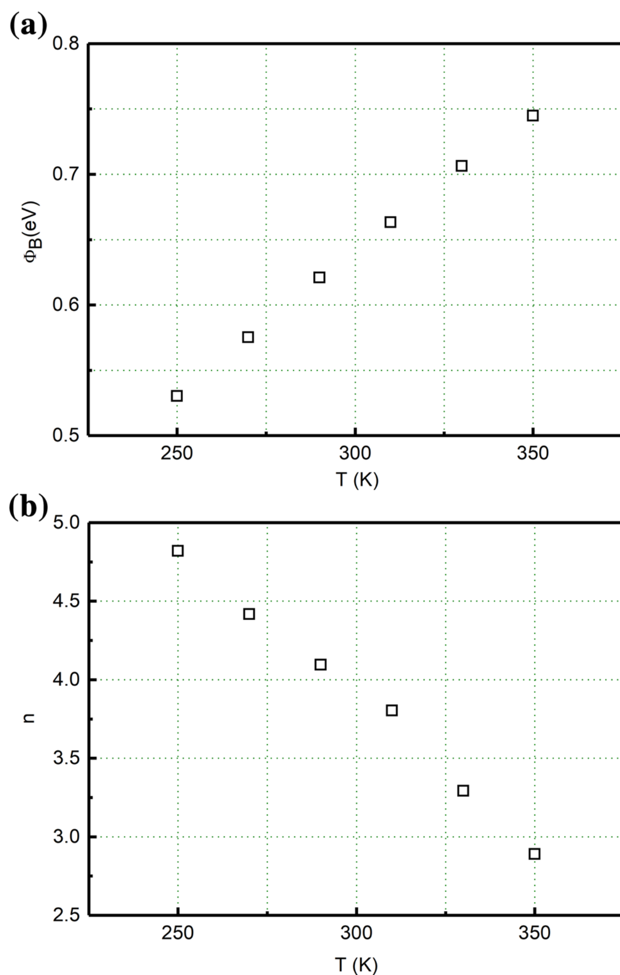

Fig. 7 Temperature dependence of **a** Φ_{B0} and **b** n for the CZTSSe/n-Si structure

[35]. The direct relation in Φ_{B0} with the change in T show that current transport across the interface is temperature activated process. As in the case of TE approximaion, when ambient temperature increases, the number of carriers having sufficient thermal energy can surmount the high barriers. On the other hand, at low temperature region they can be capable of going over the lower barriers in localized patches of barrier potential and therefore current conduction should be evaluated by considering the effect of the current flow through these patches [36, 37]. Together with the possible effects of R_s and N_{ss}, the quality of the fabricated junction is dependent to n value which is also indicative of the dominant current mechanism in the junction. Therefore, with the contribution of Eq. 3 and considering the deviation from pure TE, n can be determined from the slope of the linear region on the semi-logarithmic I–V cure given in Fig. 6 as;

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(I)}\right) \quad (5)$$

The experimental results are found in the interval of 2.89–4.82 the decrease of ambient temperature from 350 to 250 K and these values are tabulated in Table 1. These results are also shown as a function of T in Fig. 7b. For an ideal diode behavior, n should be around unity, thus it is clear that the junction is non ideal because of the higher n values. As given in Fig. 7b, Z values are inversely proportional to change in temperature and also high values can be attributed to presence of interface states at the junction and barrier inhomogeneties with low barrier patches [35]. The ideal I–V relation was modified to analyze the quality of fabricated diode and also to check the validity of pure TE model. Usually, n is expected to be in the range between 1 and 2, however, they were found higher than these values which showed that thermal excitation over the barrier was not dominant. Therefore it directed the work on the possibility of other theories from standart TE theory to explain the transport mechanism [38]. Since there was decreasing behavior in n values with the increase in the temperature, it could be evaluated as to be result of the current flow through the distribution of more low SBH patches. This observation generally depends on the structure of the junction interface that implies the inhomogeneity of the barrier height [31, 32]. In fact, the expressions for TE given in Eqs. 3, 4 were used to define the main diode parameters as Φ_{B0} and n from the experimental I–V curves. Although Eq. 3 is a general expression on I–V relationship, the validity of Eq. 4 should be evaluated on the homogeneity of barrier height formation. These variations of Φ_{B0} and n with T can be related to the consequence of a non-homogeneous barrier height formation in the junction and in this case, the higher n values from unity can be the indication of laterally inhomogeneous diode structures [38–40]. It was approximated by an examination of the degree of barrier height variation under the consideration of Tung's model and a linear relationship between Φ_{B0} and n (Fig. 8) [41]. From the extrapolation of this linear correlation to unity for n, a laterally homogeneous barrier height value was found to be about 1.10 eV for this diode structure. Since TE is based on homogeneous barrier height formation in the junction, it cannot be adequate to explain the whole carrier transport process across the junction of this fabricated diode. With the increase in n with decrease in T caused by bias dependence of the Φ_{B0} [39] small patches in Φ_{B0} can be approximated in which majority carriers are considered to go over these potential barriers if they cannot pass Φ_{B0} in order to reach the junction interface [31, 32]. The observed abnormal deviations from TE model by considering the barrier height formation can be explained by Gaussian distribution (GD) of barrier height based on a mean value, $\bar{\Phi}_{B0}$ with the standard deviation of σ_0 [31]. GD is widely used to model the potential fluctuations by assuming a continuous barrier distribution at the interface [33]. In this case, the total current is expressed with the assumption of being a sum of the current flows in all individual patches.

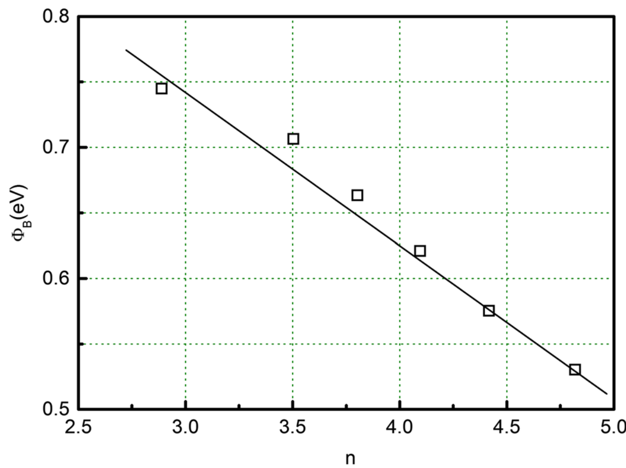

Fig. 8 Φ_{B0} vs. n plot for the CZTSSe/n-Si structure

Thus, total junction current dominated by small patches with different lower barrier heights is given as;

$$I = AA^{*}T^{2}\exp\left[\left(-\frac{qV}{kT}\right)\left(\bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT}\right)\right] \exp\left(\frac{qV}{n_{ap}kT}\right)\left[1 - \exp\left(-\frac{qV}{kT}\right)\right] \tag{6}$$

with modified reverse saturation current expression as,

$$I_0 = AA^{*}T^{2}\exp\left(-\frac{q\Phi_{ap}}{kT}\right) \tag{7}$$

where Φ_{ap} and n_{ap} are the apparent barrier height and ideality factor, respectively. Using GD function, the temperature variation of Φ_{B0} distribution can be formulated as [30, 42],

$$\Phi_{ap} = \bar{\Phi}_{B0} - \frac{q\sigma_0^2}{2kT} \tag{8}$$

As represented in Fig. 9a, Z values are in linear relation with $q/2kT$ and a linear fitting process yields $\bar{\Phi}_{B0}$ and σ_0 from the analysis of intercept and slope, respectively. The value of σ_0 is found to be 0.18 which is about 14% of the obtained $\bar{\Phi}_{B0}$ value as 1.27 eV. In this approximation of the distribution of potentials, σ_0 is a measure of the barrier homogeneity. This analysis shows that the fabricated CZTSSe/Si diode has an interfacial layer with inhomogeneities having a GD of barrier heights [43]. In GD model, the current flowing across the inhomogeneous barrier height is defined by the voltage dependent diode parameters. It is assumed that $\bar{\Phi}_{B0}$ with the standard deviation of σ_0 is linearly bias dependent with the coefficients ρ_2 and ρ_3 as given in the voltage dependent expression of n;

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{9}$$

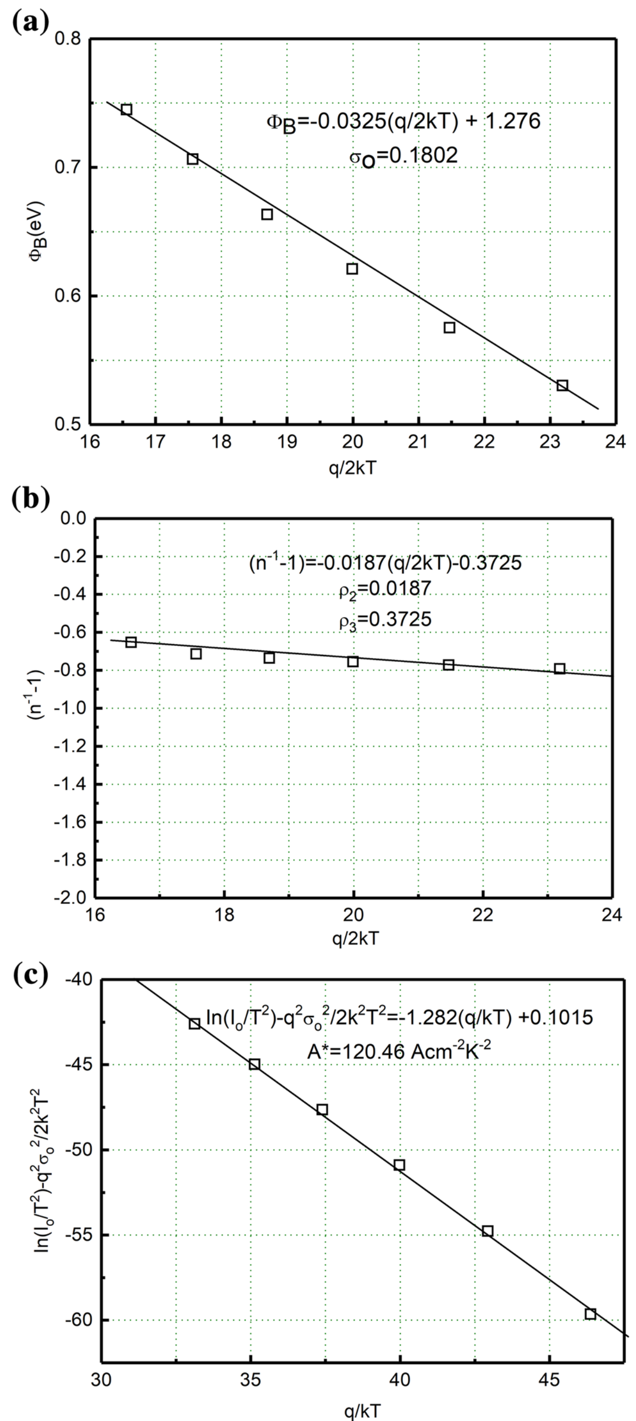

Fig. 9 Plot of **a** Φ_{B0} vs. $q/2kT$, **b** $(n^{-1}-1)$ vs. $q/2kT$, and **c** $\ln(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)$ vs. q/kT of the CZTSSe/n-Si structure

The temperature dependence of n was investigated by linear fitting of the relation given in Eq. 9. In addition, the linear relation found in Fig. 9b proves the voltage deformation of the GD of the barrier height in terms of calculated n values [38]. The voltage coefficients were calculated from the intercept and slope of the straight

line as, $\rho_2 = 0.0187$ V and $\rho_3 = 0.3725$, respectively. By applying TE model, a theoretical A^* was assumed to be applicable for this type inhomogeneous barrier height diode. However, according to the GD of barrier height, TE should be applied with the modification on A^* to reach most reasonable results of I–V analysis. Then, by using Eq. 6, modified A^* can be determined as;

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln(AA^*) - \frac{q\bar{\Phi}_{B0}}{kT} \tag{10}$$

The modified Richardson plot using Eq. 10 was given Fig. 9c. The $\bar{\Phi}_{B0}$ and A^* values were found as 1.28 eV and 120.46 A cm^{-2} k^{-2} from the slope and intercept of the $\ln(I_0/T^2) - (q^2\sigma_0^2)/(2k^2T^2)$ vs. q/kT plot, respectively. The results of Eqs. 8, 10 were found to be very close values of $\bar{\Phi}_{B0}$ and although the inhomogeneity of the barrier height was discussed in I–V analysis, the modified Richardson constant values was comparable with the reported value given in literature [28]. Moreover, the I–V characteristics for both dark and illuminated condition at room temperature are presented in Fig. 10a. As observed from figure, CZTSSe device have low response to the illumination and parameters such as open circuit voltage (V_{OC}) and short circuit current (J_{SC}) values were determined as 50 mV and 0.9 mA cm^{-2} respectively. In addition, with the help of the obtained data from the temperature dependent I–V measurement, the interface states density (D_{it}) could be obtained at the junction of CZTSSe/n-Si diode. On the condition that ideality factor is greater than unity, it can be expressed as [44],

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qD_{it}(V)\right] \tag{11}$$

where W_D is the width of space charge region, δ is the thickness of interfacial layer, ε_i and ε_s are the permittivity of insulator layer and semiconductor, respectively. (W_D values can be calculated by using capacitance–voltage characteristic). Using Eq. 11, D_{it} profile were obtained as a function of ($E_c - E_{ss}$) for various temperature values and it is given in Fig. 11. The energy interface states (E_{ss}) with respect to the top of conduction band at the surface of semiconductor is given as follows [24, 25];

$$E_c - E_{ss} = q(\phi_e - V) \tag{12}$$

where ϕ_e is the effective barrier height which is assumed to be bias-dependent due to interface state effect. As shown in the Fig. 11, D_{it} values decrease with both increasing temperature and applied voltage.

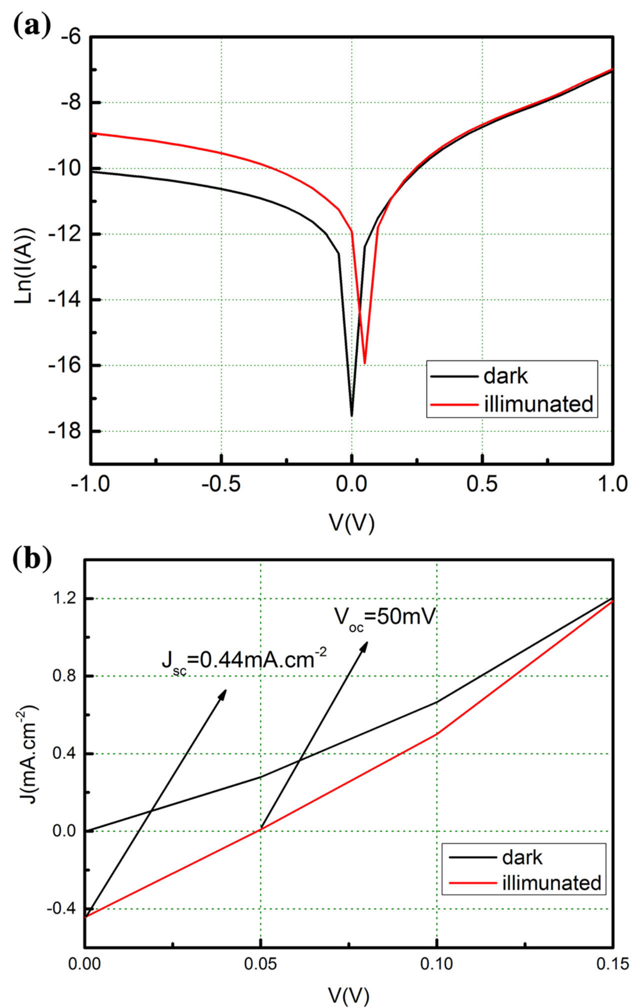

Fig. 10 **a** Room temperature I–V characteristics and **b** J–V plot at the voltage range of 0 and 0.15 V under both dark and illuminattion for CZTSSe/n-Si heterojunction structure

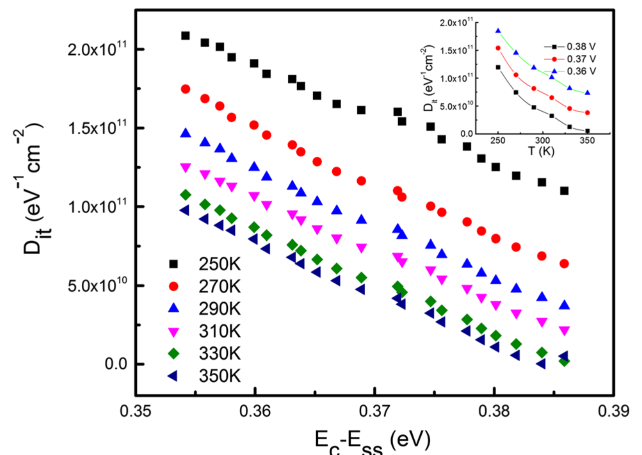

Fig. 11 The graph of the density of interface states (D_{it}) vs. ($E_c - E_{ss}$). The inset shows the variation of D_{it} with respect to voltage and temperature

3.2.2 Capacitance–voltage (C–V) analysis

To investigate the interface states density (D_{it}) of this hetero-structure, frequency dependent (C–V) and the conductance–voltage (G/w–V) measurements were carried out at room temperature. C–V and G/w–V characteristics of the CZTSSe/Si heterostructure are presented in Fig. 12a, b, respectively. As seen from the figures, the change in the frequency strongly affects C–V and G/w–V profiles of the heterojunction. There is a decrease in both capacitance and conductance with the utilizing an AC signal to junction because of the switching of majority carriers between the majority carrier band of semiconductor and interface states. At low frequencies, interface states could follow the ac signal, which leads to extra capacitance or conductance [42, 45]. Figures show that there are decreasing trends in C–V and G/w–V characteristics with increasing frequency. Additionally, a characteristic peak at the bias voltage of 0.15 V is shown as the frequency increases from 5 kHz to 1 MHz. This fluctuation could be defined in terms of the distribution of localized interface state density (D_{it}) [45].

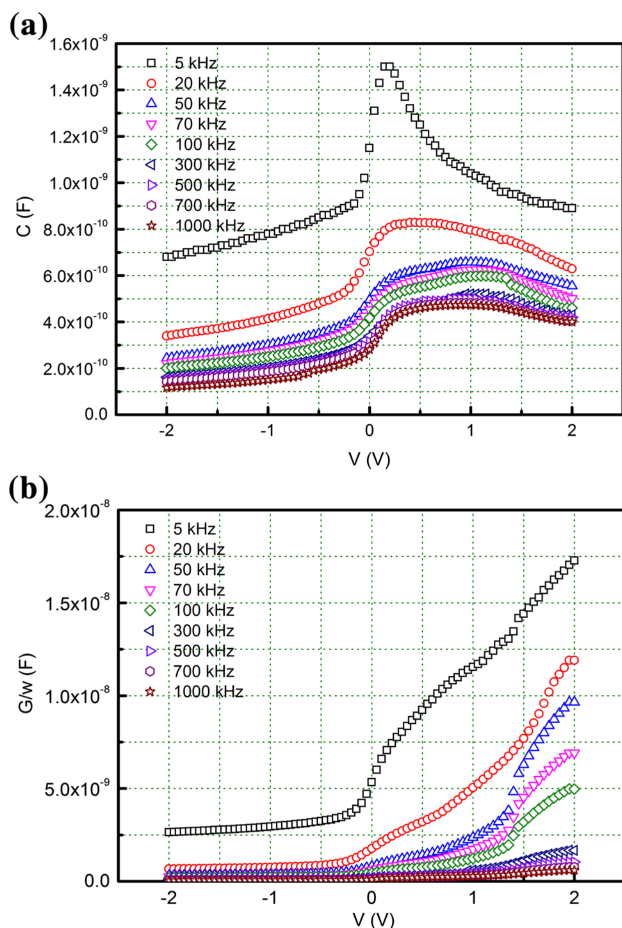

Fig. 12 **a** Capacitance–voltage and **b** conductance voltage characteristic in the frequency range of 5–1000 kHz for CZTSSe/n-Si structure

At high frequencies, on the other hand, these states could not follow the signal. To determine the interface state density, high-low frequency capacitance ($C_{HF}-C_{LF}$) and Hill–Coleman methods were used [46, 47]. The $C_{HF}-C_{LF}$ method postulates that the interface layer capacitance (C_i) is in a series connection with the parallel connection of the interface state capacitance (C_{it}) and the space charge capacitance (C_{sc}). Interface state capacitance can be described as follows;

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_i} \right)^{-1} - C_{sc} \tag{13}$$

Surface states cannot respond to ac signal at high frequencies, and thus, total capacitance does not include these states. For this reason, equivalent capacitance is defined by the series connection of C_i and C_{sc} and given as,

$$\frac{1}{C_{HF}} = \frac{1}{C_i} + \frac{1}{C_{sc}} \tag{14}$$

Thus, the interface states density (D_{it}) at a given bias could be obtained by combining Eqs. (13) and (14);

$$qAD_{it} = C_{it} = \left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i} \right)^{-1} \left(\frac{1}{C_{HF}} - \frac{1}{C_i} \right)^{-1} \right] \tag{15}$$

where A is the active diode area, C_{HF} and C_{LF} are the measured highest frequency capacitance (1 MHz) and lowest frequency capacitance (5 kHz), respectively. The distribution of the interface state density D_{it} of for CZTSSe/Si heterostructure is given in Fig. 13a. It can be seen that the value of D_{it} has a peak around 0.15 V. This peak could be related with the extra capacitance peak in the C–V characteristic discussed above. In addition, Hill–Coleman method was applied to explain the behavior of D_{it} more explicitly and D_{it} was expressed as [48];

$$D_{it} = \left(\frac{2}{qA} \right) \frac{(G_m/w)_{\max}}{\left[(G_m/w)_{\max}/C_i \right]^2 + (1 - C_m/C_i)^2} \tag{16}$$

Figure 13b shows the frequency dependent Dit profile of CZTSSe/Si heterostructure calculated by the Hill–Coleman method. As seen from the figure, D_{it} values have a decreasing trend with the increasing frequency. The decreasing of the Dit values at higher frequencies shows that these states are not able to follow ac signal at high frequencies. Thus, it is seen that the interface state density values determined by two different methods are approximately the same order. Besides, these values are close to the values of D_{it} calculated with the temperature dependent I–V measurement.

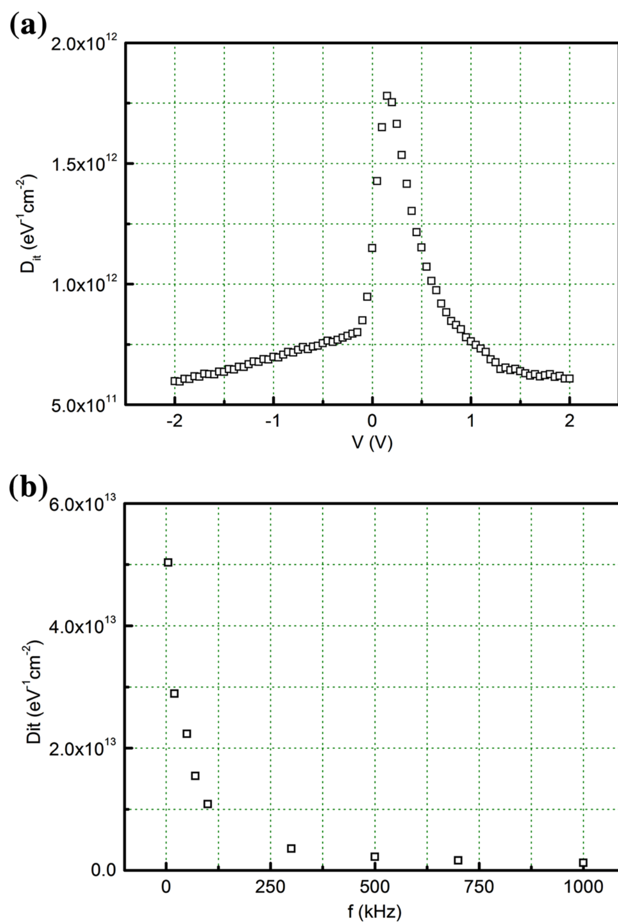

Fig. 13 Density of interface states profiles obtained from **a** $C_{HF} - C_{LF}$ capacitance method and **b** Hill–Coleman method

4 Conclusion

In summary, material characterization of deposited films were determined by using the samples deposited on glass substrates. The films deposited on SLG substrates were indicated Cu poor, Sn rich compositions and they were in polycrystalline nature along with (112) preferred orientation direction. However, from XRD and Raman measurements, secondary phases were also detected. Deposited CZTSSe thin films showed direct optical transition with 1.46 eV band gap energy and p-type semiconductor behavior. From the dark current–voltage characteristics in wide temperature range, main diode parameters were calculated by thermionic emission model and the results revealed the decreasing barrier height and the increasing ideality factor behavior with decreasing temperature, which could be the results of the barrier height inhomogeneity at the interface. Thus, the inhomogeneity at the interface was explained by Gaussian distribution of barrier heights. Under this approximation, mean barrier height height ($\bar{\Phi}_{B0}$) and standard deviation (σ_0) at zero bias were found to be 1.27 eV and 0.18 V, respectively. By means of modified Richardson plot, Richardson constant was calculated as 120.46 A cm^{-2} k^{-2} which was close to theoretical value known for n-Si. Effects of the illumination on the device was characterized by I–V measurement under AM 1.5 condition, and from illuminated I–V curve, V_{OC} and J_{SC} values were calculated as 50 mV and 0.9 mA cm^{-2}, respectively. In addition, using frequency dependent capacitance–voltage characteristics CZTSSe/Si structure, the density of interface state profiles were obtained by means of high-low frequency capacitance and Hill–Coleman methods.

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