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Study on the electrical properties of ZnSe/Si heterojunction diode

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Abstract ZnSe thin film is e-beam evaporated on monocrystalline p-Si to fabricate n-ZnSe/p-Si heterojunction. The electrical properties were investigated by current–voltage (I–V), capacitance–voltage (C–V) and conductance–voltage (G/w–V) measurements. The forward bias I–V characteristics were analyzed in the temperature range of 220–360 K. The fabricated diode structure exhibited rectifying characteristics with a two order rectification ratio. The current transport in the junction was modeled by the modification of thermionic emission (TE) in which the observed anomaly was related to the interfacial disorder at the junction. From this analysis, the zero-bias barrier height and ideality factor at room temperature condition were determined as 0.775 and 3.195 eV, respectively. The TE anomaly was also evaluated by considering the fluctuations due to the barrier inhomogeneity and the assumption of Gaussian distribution in barrier height. Therefore, the forward bias I–V results were used to determine the density of interface states. The frequency dependence of C–V and G/w–V characteristics of the n-ZnSe/p-Si heterostructure were studied by taking into account of the effect of the series resistance and interface states at room temperature. According to the high-low frequency capacitance and Hill-Coleman methods, density of interface states was calculated and these experimental values were found in decreasing behavior with increasing frequency. The voltage and frequency dependence of series resistance values obtained from C–V and G/w–V measurements were also related to the insulator layer and the distribution density of interface states.

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1 Introduction

Family of II–VI semiconductor compounds have been figured out a wide range of material properties in applications of optoelectronics with showing from narrower as 0–3.7 eV wide band gap values [1]. It is also expected to provide a variety of electronic applications with their high iconicity characteristics [1, 2]. Among these compounds, zinc selenide (ZnSe) is an intrinsic n-type semiconductor with a band gap of about 2.7 eV [1–5]. It is transparent over a wide range of the visible spectrum and attracts the applications of devices operation in this optical region of interest [3, 6] In addition to its material characteristics, offering low cost and high quality as in thin film layer in device applications, it has been generated a great deal of interest in the applications of thin film devices [5–8] In the literature, Si based binary thin film heterojunction diodes have gained much attentions [9, 10], however, there are limited experimental and theoretical works on the ZnSe heterojunction with Si [11–15]. In these literature works, the dominant current transport mechanism in the ZnSe/Si junction in which ZnSe layer were deposited by vacuum evaporation [11] and sputtering methods [12], was reported as space-charge-limited current mechanism (SCLC). Electron affinity of this structure was approximated as to be 4.09 eV and thus, the diode parameters were reported as 3.8 and 0.87 eV for vacuum deposited in ideality

factor (n) and potential barrier height (∅), respectively [11] and they were given in the intervals of 2–5 and 0.55–0.66 eV for sputtered diode [12]. Additionally, another work on vacuum evaporated ZnSe diode was analyzed under the effect of interfacial layer between the metal and the semiconductor, and the junction current was modeled as the combination of the thermionic current and the recombination current [13]. In this reported work, n and ∅ were characterized as a function of temperature and they were found as 2.8 and 0.61 eV at room temperature, respectively. In addition to the junction with bare Si, ZnSe nanowire (NW)/Si p–n diode structures were fabricated and the I–V characteristics were analyzed from the ohmic contacts of Cu/Au electrodes with NWs [14]. These heterojunctions with good rectifying characteristics were presented with $n = 1.95$ and ∅=0.91 eV [4]. On the other hand, the theoretical work on this type of diode structure was focused on the principles of the ZnSe/Si core–shell NW heterostructures, and related parameters were calculated by density functional theory (DFT) [15].

In this work, ZnSe thin film layer was deposited on polished mono-crystalline p-Si wafer substrate by e-beam evaporation technique, which is simple and reproducible way in the methods used to reach high-quality film structure. Experimental investigation was focused on current–voltage (I–V) and capacitance–voltage (C–V) measurements and the analyses were carried out to characterize the electrical properties of n-ZnSe/p-Si diode.

2 Experimental details

In this work, ZnSe film layer was evaporated by high energetic electron beam directed to the stoichiometric ZnSe powder source on the graphite crucible in a vacuum of 10^{-6} Torr using a high vacuum coating unit. This method with a localized heating on the source material provides uniform high-purity thin film deposition. The substrate temperature was kept constant at 200 °C and the deposition rate was controlled at about 3 Å/s. The rate and thickness values were monitored by Inficon XTM/2 deposition monitor and the final thickness was measured by Vecoo Dektak 6 M thickness profilometer. The n-ZnSe/p-Si heterostructure was fabricated by depositing ZnSe film layer on (111) crystal oriented p-type Si wafer with the resistivity value of 1–10 (Ω cm). Before deposition processes, Si substrates were dipped in $HF:H_2O$ solution to remove native oxide. In order to complete the diode structure, the back ohmic contact on the Si wafer was formed by elemental Al evaporation and post-annealing treatment at 450 °C under the nitrogen atmosphere. In addition, top ohmic contact layer onto ZnSe film surface was deposited by thermal evaporation of In in circular dot contact shape of 2 mm diameter and around 200 nm thickness; then the complete structure was annealed at 100 °C under the nitrogen atmosphere to enhance the ohmicity of the contacts. Additionally, material properties of the deposited film structure were investigated by the fabrication of ZnSe layer on the ultrasonically and chemically cleaned soda-lime glass substrate in the same deposition cycle. Atomic composition of the film sample was determined by Quanta 400F field emission scanning electron microscope (SEM) equipped with energy dispersive X-ray spectroscopy (EDS). The X-ray diffraction profile of the deposited films were investigated by Rigaku Miniflex X-ray diffraction (XRD) system equipped with Cu-Kα X-ray source ($\lambda = 1.54$ Å) and the surface topography of the film was observed by Veeco MultiMode V, atomic force microscope (AFM). Spectral transmission was measured by using Perkin–Elmer Lambda 45 spectrophotometer in the 300–1100 nm wavelength region.

The diode characteristics were analyzed by temperature dependent current–voltage (I–V) and room temperature capacitance–voltage (C–V) measurements. Keithley 2401 source-measure unit was used and the sample temperature was scanned from 220 to 360 K by the help of CTI-Cryogenics Model 22 refrigerator system combined with Model SC helium compressor. In this measurement system, the temperature of the sample was controlled and monitored by using Lakeshore DRC-91C controller. The frequency dependent C–V measurements were carried out with the computer-controlled system by using Hewlett Packard 4192A LF model impedance analyzer.

3 Results and discussions

The material properties of ZnSe thin film layer were investigated by using the samples deposited on glass substrates. EDS was used to quantify the constituent elements in the ZnSe film, and it was found in stoichiometric composition with a 1:1 molar ratio of Zn:Se elements without any elemental impurity contribution. The film thickness was measured by the thickness profilometer as about 500 nm. From XRD diffractogram given in Fig. 1, ZnSe thin film is in polycrystalline structure along (111) orientation direction and demonstrates the crystallization in cubic zinc-blende structure [11, 13].

The surface morphology of this layer was characterized by AFM measurements. It was observed as homogeneous and crack-free surface morphology (Fig. 2) and the measured surface roughness is almost uniform with the value of 2.5 nm.

Figure 3 shows the spectral behavior of the ZnSe layer and the optical transmission values of the films were found in between 80 and 90% in the optical transparent region. From transmission values, the absorption coefficient of the film was calculated by using the expression;

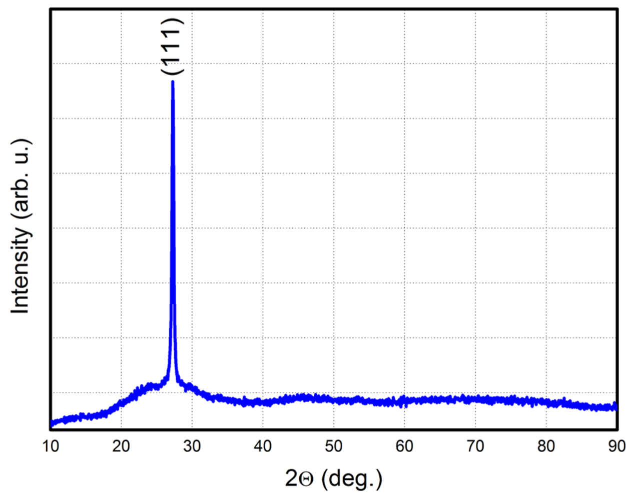

Fig. 1 XRD profile of the deposited ZnSe film

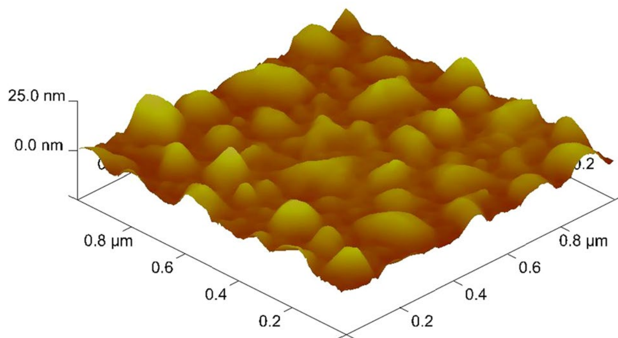

Fig. 2 AFM image of the deposited ZnSe film layer

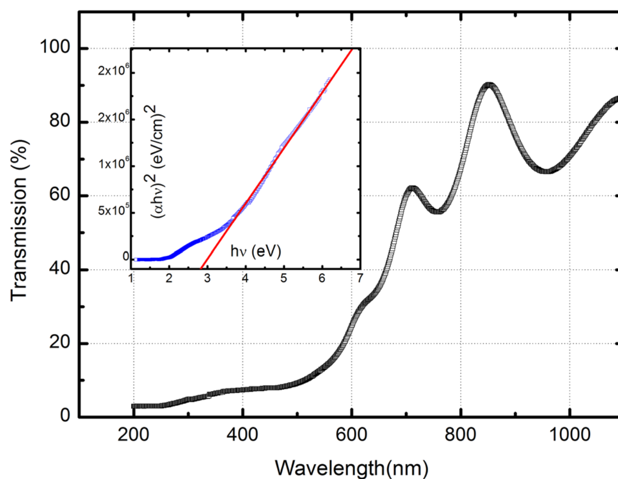

Fig. 3 Transmission spectrum and Tauc plot (*inset*) of the deposited ZnSe film layer

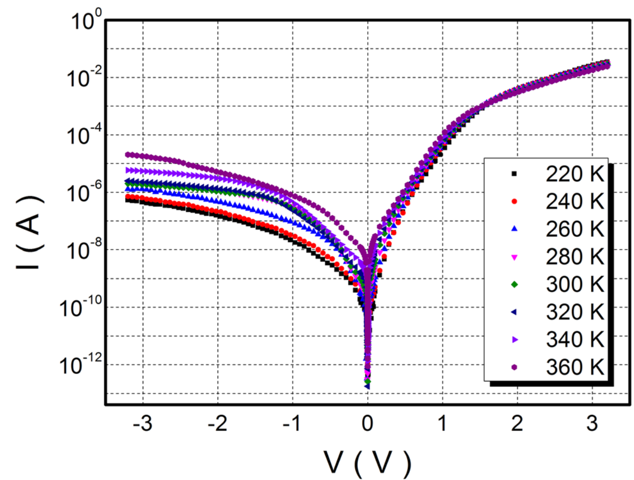

Fig. 4 Semi-logarithmic I–V plot of n-ZnSe/p-Si heterojunction at different ambient temperatures

$$\alpha = \frac{1}{d}\ln(T) \tag{1}$$

The band gap value of the ZnSe film was determined by using the calculated absorption coefficient value versus photon energy ($h\nu$) plot as,

$$\alpha h\nu = A(h\nu - E_g)^{1/2} \tag{2}$$

From Tauc plot given in Fig. 3 (inset), the fundamental band gap value is obtained as about 2.8 eV and the result is consistent with the reported value [16].

3.1 Current–voltage analysis

The temperature dependent current–voltage (I–V) analysis was carried out under dark condition to determine the electrical parameters of the ZnSe/Si diode. The experimental forward and reverse bias I–V characteristics of the diode carried out at the ambient temperature range of 220–360 K was presented as semi-logarithmic I–V plot in Fig. 4. From this figure, the rectifying behavior in I with V can be evaluated as an indication of a typical p–n junction diode [17] and shows as about two order in magnitude of rectification factor (ratio of forward to reverse current).

In the I–V analysis, according to the origin of pure thermionic emission (TE) theory, the current through the junction barrier at forward bias region can be expressed as,

$$I = I_0\left[\exp\left(\frac{qV}{kT}\right) - 1\right] \tag{3}$$

where I_0 is the reverse-saturation current, q is the electronic charge, V is the voltage value in the forward bias region, k is the Boltzmann constant and T is the ambient temperature (in

the unit of K) during the measurement. Apart from the ideal case, taking into consideration of the experimental work, ideality factor, n can take the value different from unity and therefore, the deviation from ideality can be inserted to the modified equation as,

$$I = I_0\left[\exp\left(\frac{qV}{nkT}\right) - 1\right] \quad (4)$$

As shown in Fig. 4, the I–V curve deviates from linear behavior above the bias voltage of 2.0 V. This current behavior is the result of the series resistance (R_S) effect and interface states (D_{it}) dominant at the high forward bias region [18]. Under these saturation effects, experimental I–V characteristics of the diode deviate from the ideal case. Therefore, in experimental work, standard I–V relation according to TE model should be re-evaluated in terms of the effects of the series resistance and voltage factor can be shared on the R_S and the diode. In this case, applied bias term, V in Eq. 4 can be written as $V_D + IR_s$, with the bias voltage across the diode (V_D), and R_S (IR_s). In the formation of device applications, it is expected to be low enough to minimize the voltage drop across R_S, however, it was accepted as zero in ideal case. In fact, R_S can be occurred due to the resistance effects of both diode structure and contact regions [19], and interface state effects may be observed on unintentional oxidized surfaces in the junction [20]. This assumption is valid at the high forward bias region and accepted to be negligible in the linear part of I–V under consideration of superiority betweenV_D and IR_s.

For the fabricated diode, I_0 values were obtained from the intercept value of ln*(I)* at zero bias of the straight line region on I–V curve, at each temperature step and given in Table 1. In fact, I_0 can be expressed as,

$$I_0 = AA^*T^2 \exp\left(-q\emptyset_{b0}/kT\right) \quad (5)$$

where A is the effective diode area and A^* is the effective Richardson constant, $\emptyset_{b0}$ is the barrier height at zero bias point. With TE assumptions, A^* can be described according to the nearly free electrons in vacuum as the following relation,

$$A^* = 4\pi m^* k^2/h^3 = 120(m^*/m) \quad (6)$$

with Planck constant, h, mass of majority carrier m and its constant effective mass value m^* [21] Then, this parameter can be simplified as 32 A/cm^2 K^2 to approximate the diode calculations [22].

Together with R_S, the quality of the fabricated junction is dependent to n value which is also indication of the dominant current transport mechanism in the junction. From the modified I–V relation given in Eq. 4, the n values can be obtained as,

$$n = \frac{q}{kT}\left(\frac{dV}{d\ln(I)}\right). \quad (7)$$

By using Eq. 7, the experimental values were deduced from the slope of the linear region of Fig. 4 and the results were also given in Table 1. As listed in Table 1, the values are inversely proportional to change in temperature and also high value of ideality factor can be attributed to presence of interface states at the junction and barrier inhomogeneity with low barrier patches [23, 24].

By using the theoretical approach, zero-bias barrier height, $\emptyset_{b0}$ can be obtained from the I_0 values as,

$$\emptyset_{b0} = \frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_0}\right) \quad (8)$$

In this calculation, experimental $\emptyset_{b0}$ values were estimated at each temperature according to the Richardson constant of p-Si layer [22]. The calculated values were listed in Table 1 and they were found in increasing behavior with increase in T, because of the free carriers having enough energy to surmount the barriers and they have the contribution to the conduction with increasing T [25].

The ideal I–V relation was modified to analyze the quality of fabricated diode and also to check the validity of pure TE model. Usually, n is expected to be in the range between 1 and 2, however, they were found higher than these values which implies that thermal excitation over the barrier is not dominant. Therefore it directs the work on the possibility of other theories to explain the transport mechanism [17]. The n values varying with temperature can be described with the linearity of n versus *1/T* plot (Fig. 5) by assuming the particular distribution of surface states in the diode structure [26]. A small deviation in the ideality factor in this temperature region is thought to be caused by the higher value of the ideality factor characterized by the current flow through the distribution of more low SBH patches [27, 28]. The temperature dependence of ideality factor indicates that the observed values need to be considered over the TE. Thus, the current transport

Table 1 Diode parameters calculated by applying TE theory

T (K)	Ideality factor (n)	Saturation current (I_0) (A)	Barrier height ($\emptyset_{b0}$) (eV)	Interface states (D_{it}) (eV^{-1} cm^{-2})
220	3.8	2.24×10^{-10}	0.61	1.53×10^{13}
240	3.6	3.36×10^{-10}	0.66	1.45×10^{13}
260	3.5	6.99×10^{-10}	0.69	1.37×10^{13}
280	3.2	8.80×10^{-10}	0.75	1.24×10^{13}
300	3.2	2.32×10^{-9}	0.78	1.21×10^{13}
320	3.0	2.97×10^{-9}	0.82	1.10×10^{13}
340	2.8	3.87×10^{-9}	0.86	1.00×10^{13}
360	2.7	7.94×10^{-9}	0.89	9.40×10^{12}

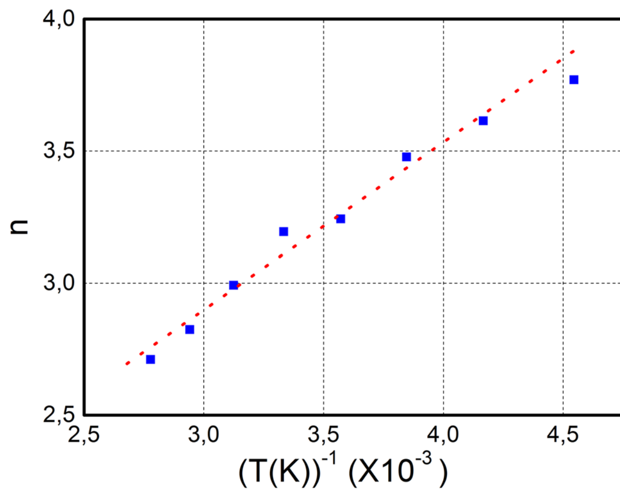

Fig. 5 Variation of ideality factor with sample temperature for ZnSe/Si structure

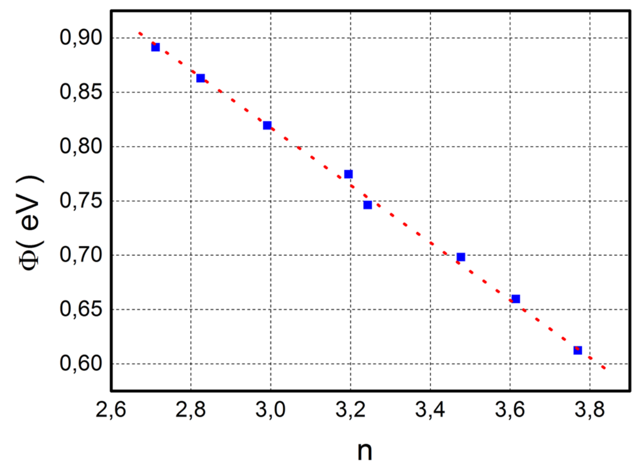

Fig. 6 Barrier height versus ideality factor for ZnSe/Si structure

mechanism in the junction was evaluated with the modified thermionic emission transport model expressed as,

$$n(T) = n_0 + \frac{T_0}{T} \tag{9}$$

where T_0 is a constant independent of temperature, however it is affected by applied bias voltage [29]. This model is the modification of TE with T_0, and this anomaly is related to the interfacial disorder at or near the junction. From the slope and intercept analyses, the relation between n and inverse temperature gives the parameters n_0 and T_0 as 1.089 and 604.64 K respectively.

It was shown that the TE anomaly can be also connected with the lateral inhomogeneity of the barrier height as analyzing the changes in n and $\emptyset_{b0}$ values [30, 31]. The same behavior of the ideality factor was observed in the literature and has been interpreted in terms of interface state density distribution [32].

As given in Table 1, with increasing temperature, $\emptyset_{b0}$ decreases and n increases. These variations with T might be the consequence of a non-homogeneous barrier height formation in the junction. The n values higher than unity was evaluated as laterally inhomogeneous diode structures [33]. It was approximated by an examination of the degree of barrier height variation under the consideration of Tung's model and a linear relationship between $\emptyset_{b0}$ and the n [34, 35]. This inverse linear relation between $\emptyset_{b0}$ and n was presented in Fig. 6. This observation further indicates that the conduction mechanism operating in the junction seems most likely T_0 effected current transport mechanism across the junction in the whole temperature region. From the extrapolation of this linear correlation to $n=1$, a laterally homogeneous barrier height value was found to be about 1.34 eV for this structure [34].

The obtained anomaly in TE theory for this junction can be analyzed by considering the fluctuations due to the barrier inhomogeneity and suggesting Gaussian distribution in barrier height, $\emptyset_b(V)$. In this approach, the diode with $\emptyset_b$was approximated to be made of parallel diodes with different barrier heights which effect the current transport in the junction independently [36, 37]. This Gaussian distribution can be formulated as,

$$\emptyset_{ap} = \bar{\emptyset}_{b0} - \frac{q\sigma_s^2}{2kT} \tag{10}$$

where $\emptyset_{ap}$ is the apparent barrier height from the modified barrier height expression [38], $\bar{\emptyset}_{b0}$ is the mean value and σ_s is the standard deviation in the T dependence of barrier height. In fact, σ_s is used to measure the deviation from the homogeneity of barrier height in the junction [39]. The $\emptyset$ versus $q/2kT$ (Fig. 7) indicates the expected linear relation given in Eq. 10 and from the intercept and slope, $\bar{\emptyset}_{b0}$ and σ_s were calculated.

Moreover, this assumption can be related with the ideality factor n with the distribution functions in barrier height expression. The barrier distribution at all bias voltages can be described by a Gaussian distribution; therefore the voltage effect in n values can be formulated by the bias dependent Gaussian coefficients as,

$$\left(\frac{1}{n_{ap}} - 1\right) = -\rho_2 + \frac{q\rho_3}{2kT} \tag{11}$$

In this relation, n_{ap} is the voltage independent, apparent ideality factor used to describe the barrier distribution [38], ρ_2 and ρ_3 are the parameters to express the bias dependence of $\bar{\emptyset}_{b0}$ and σ_s, respectively. These parameters are used as the identification of the voltage deformation

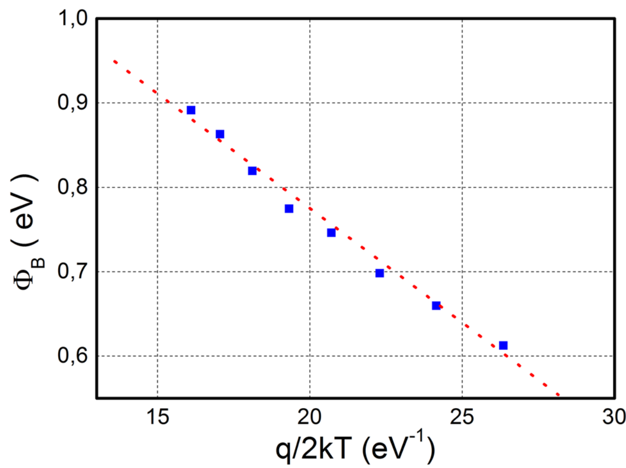

Fig. 7 Plot of barrier height versus $q/2kT$

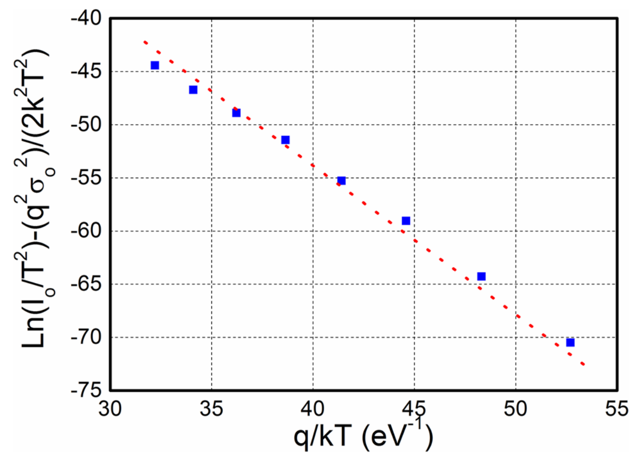

Fig. 9 $\{\ln\left(I_0/T^2\right) - q^2\sigma_0^2/2k^2T^2\}$ versus q/kT for the ZnSe/Si structure

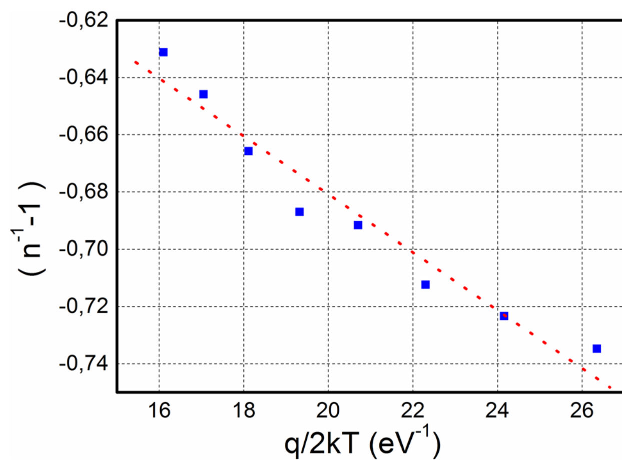

Fig. 8 Plot of $(n^{-1} - 1)$ versus $q/2kT$ of the ZnSe/Si structure

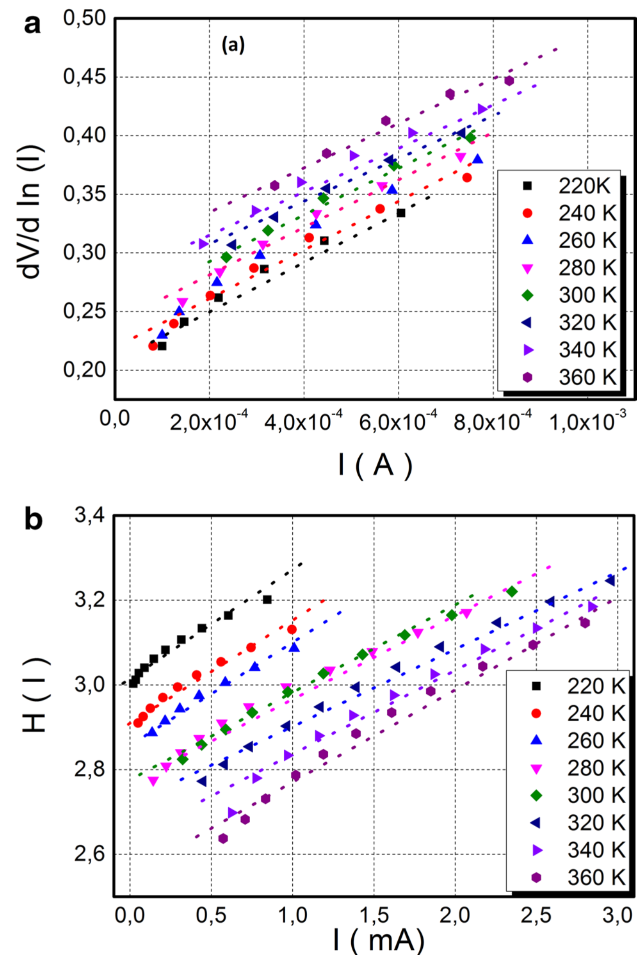

Fig. 10 $dV/d(\ln I)$ versus I (**a**) and$H(I)$ versus I (**b**) plots of ZnSe/Si structure

of the barrier height distribution. In fact, Eq. 11 predicts the temperature effect on n and it is used as a measure for the homogenization of the barrier distribution [38, 39].

From the linear relation observed in Fig. 8, the voltage coefficients were calculated from the slope and intercept as, $\rho_2 = 0.4803$ V and $\rho_3 = 0.0101$, respectively. In addition, the experimental way to obtain the actual Richardson constant for this studied sample is using the result of Gaussian distribution of barrier height with the expression [40] as,

$$\left(\frac{I_0}{T^2}\right) - \left(\frac{q^2\sigma_s^2}{2k^2T^2}\right) = \ln\left(AA^*\right) - \frac{q\bar{\emptyset}_{b0}}{kT}$$

The modified I–V relation under the assumption of Gaussian distribution was presented in Fig. 10. The slope of the straight line directed to $\bar{\emptyset}_{b0}$ and extrapolation value

was used to determine A^* for a given diode area, A. The results of Figs. 8 and 9 were found to be very close values of $\bar{\emptyset}_{b0}$ as about 1.32 eV. Although it was different than theoretical value, A^* was calculated in the order of the reported work, [41] as 32.2 A/cm^{2}K^2.

The series resistance of the diode was calculated with using the technique proposed by Cheung and Cheung [42, 43]. Under the effect of series resistance, Cheung's function developed on forward bias I–V characteristics is given as,

$$\frac{dV}{d(\ln I)} = IR_s + n\left(\frac{kT}{q}\right) \tag{13}$$

where this expression is the modified version of Eq. 7 in terms of R_s, and

$$H(I) = V - n\left(\frac{kT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = n\emptyset_{b0} + IR_s \tag{14}$$

With these equations, it is expected that both of $dV/d(lnI)$ versus I and $H(I)$ versus I plots should be in straight line behavior. Figure 10 shows linear characteristics for the data of downward curvature region in the forward bias I–V. According to Eq. 13, R_s values were calculated from the slope of Fig. 10a and the determination of these resistance values were also checked from the slope of Fig. 10b by using Eq. 13. In fact, the Cheung's theory was applied to the experimental data with Eq. 14 and plotted in Fig. 11a; additionally, the consistency of this approach was analyzed with Eq. 14 from the relation presented in Fig. 10b.

The obtained R_s values from the slope of both of these plots were presented in Fig. 11. As given in this figure, the results are in a good agreement with each other.

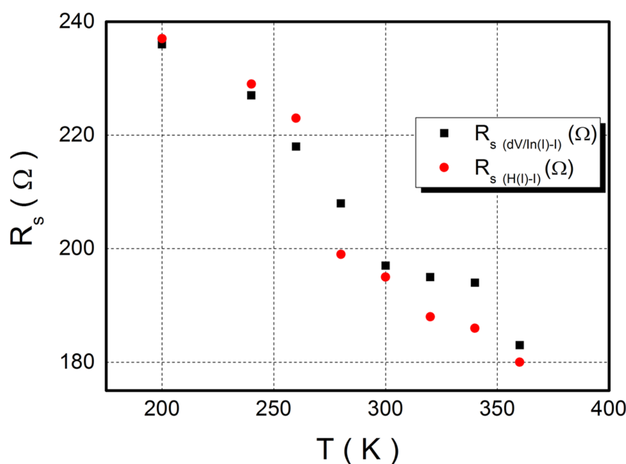

Fig. 11 Plot of temperature dependent series resistance values for ZnSe/Si structure

3.2 Capacitance–voltage analysis

The frequency dependent capacitance–voltage (C–V) and the conductance–voltage (G/w–V) measurements for the ZnSe/p-Si at room temperature are presented in Fig. 12a and b, respectively. As seen from the Fig. 12a, the change in the frequency is ineffective in the C–V characteristic of the heterojunction, but Fig. 12b indicates that the G/w–V characteristic is strongly dependent on frequency.

Applying a small AC signal to device lead to decrease in conductance due to the switching of majority carriers between the majority carrier band of semiconductor and interface states. This interface states could follow the ac signal at low frequencies which lead to extra capacitance or conductance. On the other hand, at high frequencies these states are not able to follow the signal and the peak due to the extra conductance has a missing trend [39, 44]. Figure 12b reveals that, there is a sharp decrease in G/w and it gives a characteristic peak at the bias voltage of −2 V when the frequency increases from 1 kHz to 1 MHz. The distribution of localized interface state density (D_{it}) could

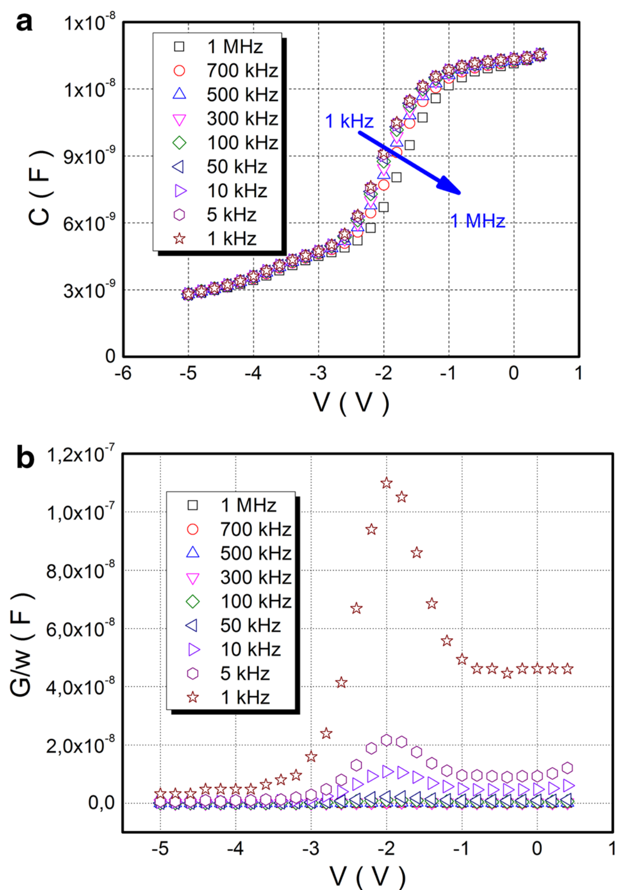

Fig. 12 Capacitance *(C)* and conductance *(G/w)* versus bias voltage at room temperature (**a**) and various frequencies (**b**) for ZnSe/Si structure

be influential for this observed fluctuation [45]. In order to determine the interface state density *(D_{it})*, both high-low frequency capacitance (C_{HF}–C_{LF}) and Hill-Coleman methods were used [45–47]. According to the method of C_{HF}–C_{LF}, the interface layer capacitance (C_i) is in a series connection with the parallel connection of the interface state capacitance (C_{ss}) and the space charge capacitance (C_{sc}). Thus, the interface states densities *(D_{it})* at a given bias could be obtained by;

$$D_{it} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{}{C_i}\right)^{-1}\left(\frac{1}{C_{HF}} - \frac{}{C_i}\right)^{-1}\right] \tag{15}$$

where C_{HF} *and* C_{LF} symbolize the measured highest frequency capacitance (1 MHz) and lowest frequency capacitance (1 kHz), respectively [45].

Figure 13 illustrates the applied voltage dependence of D_{it} values obtained from the C_{HF}–C_{LF} method. As seen from this figure, D_{it} values are increasing with the applied bias and there is no any other peak. This could be the indication of the continuum or bands of interfacial states [48]. On the other hand, D_{it} behavior might be subjected to many components such as, the magnitude of the voltage, frequency, fabrication process of the junction, homogeneity of interfacial layers [49].

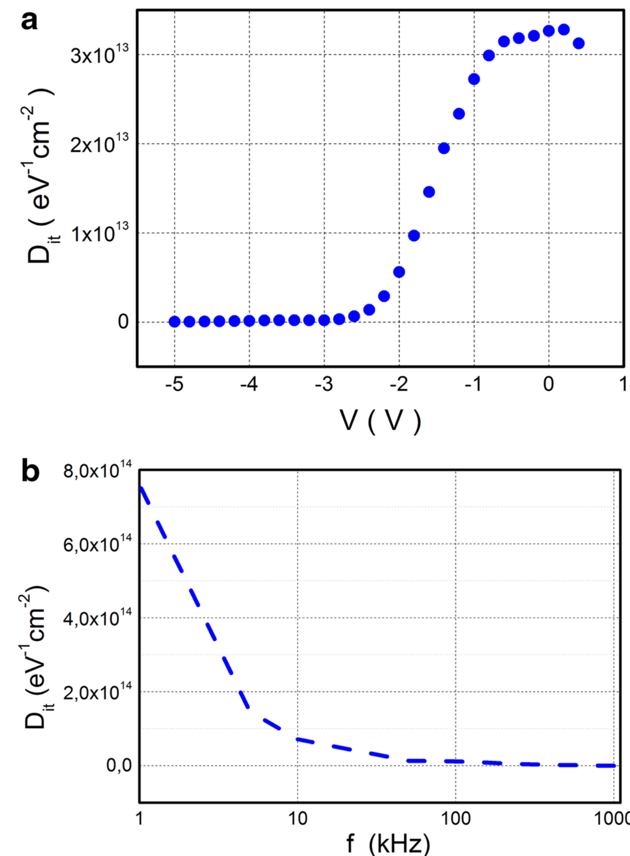

Fig. 13 Interface state characteristics in ZnSe/Si diode in terms of **a** C_{HF}–C_{LF} and **b** Hill-Coleman method

In order to explain D_{it} behavior more explicitly, the frequency dependence distribution of D_{it} values was obtain due to *Hill-Coleman* method; [47, 50]

$$D_{it} = \left(\frac{2}{qA}\right)\frac{(G_m/w)_m ax}{(((G_m/w)_m ax/C_i)^2 + (1 - C_m/C_i))^2} \tag{16}$$

The frequency dependence D_{it} behavior is given in the inset of Fig. 13b and it shows that D_{it} values decreases with increasing frequency. The decline in the D_{it} values at higher frequencies indicates that these states are not able to follow ac signal at high frequencies [17]. Thus, it can be concluded that the results obtained from C_{HF}–C_{LF} and *Hill-Coleman* methods are well-matched.

Additionally, the forward bias I–V results can be used to determine the D_{it} values by considering the interface states in equilibrium with the semiconductor [51, 52]. In the non-ideal diode behavior in which the values of *n* greater than the unity, this behavior can be expressed as,

$$n(V) = 1 + \frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{w_D} + qD_{it}\right) \tag{17}$$

where w_D is the width of the space charge region, ε_i and ε_s are the permittivity of interfacial insulator and semiconductor layers, respectively [53, 54]. Thus, D_{it} values were calculated as a function of $E_{ss} - E_V$ values. In this energy parameter, E_{ss} is defined as the energy of the interface states from the top of the valence band at the semiconductor surface, and it is given by,

$$E_{ss} - E_V = q(\Phi_e - V) \tag{18}$$

with the effective barrier height Φ_e being a voltage dependent parameter with the possibility of an interface states in the diode structure [53].

The calculated D_{it} values were listed in Table 1 and illustration in terms of ($E_{ss} - E_V$) is given in Fig. 14. As seen in Fig. 14, the experimental data is found in decreasing behavior with increasing *T*. This can be resulted from the molecular restructuring and reordering of the interface under the effect of temperature [51, 54].

Series resistance (R_s) value is also as important as the values of D_{it} which affect the device performance. To get the voltage and frequency dependence of R_s values, admittance method was used [55]. This method provides the determination of R_s for reverse and forward bias regions, and R_s values are given as,

$$R_s = \frac{G_m}{G_m^2 + w^2 C_m^2}. \tag{19}$$

The values of R_s can be calculated from the C–V and G/w–V data in various frequencies. The voltage dependence

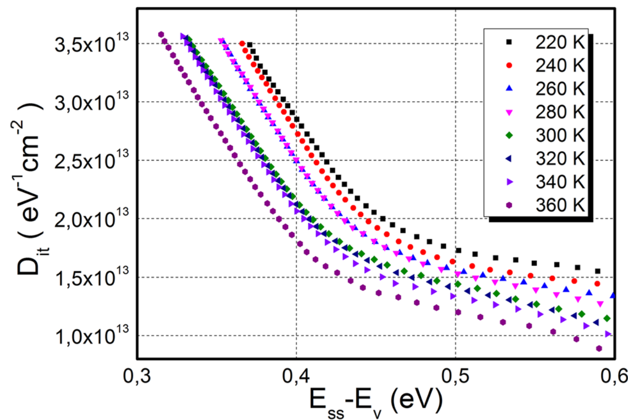

Fig. 14 Plot of density of interface states, D_{it} versus $E_{SS}-E_V$ obtained from the I–V measurement

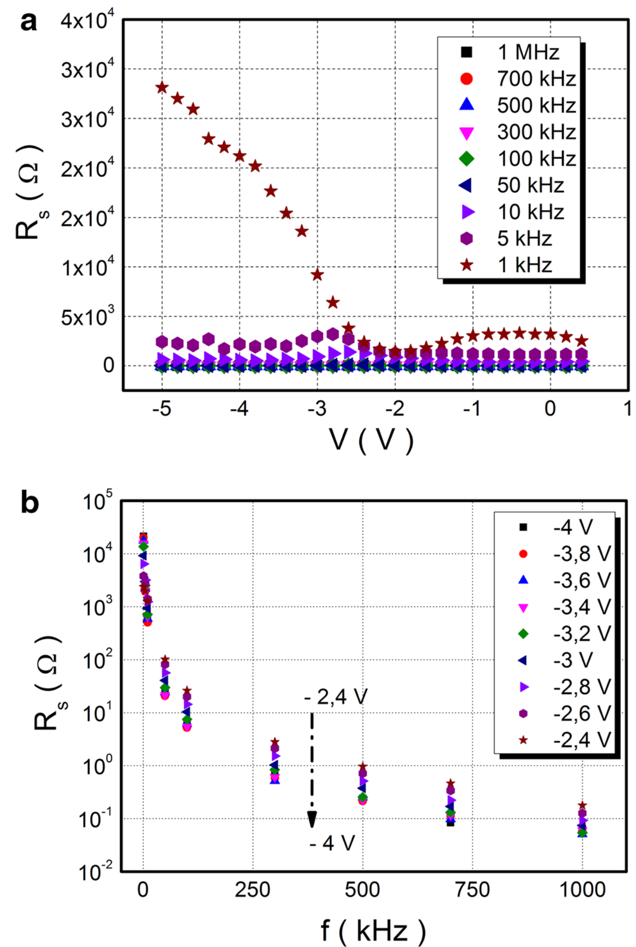

Fig. 15 Voltage (**a**) and frequency (**b**) dependencies of series resistance for ZnSe/Si structure

of R_s for the ZnSe/Si structure at the frequency range from 1 kHz to 1 MHz at room temperature is plotted in Fig. 15. As seen Fig. 15a, the R_s gives peak depending on frequency in the voltage range from −5 to 0.4 V and the value of R_s is decreasing with increasing frequency. Therefore, special attention should be given to the effects of the R_s in the applications of the admittance-based measured methods (C–V and G/w–V) [56, 57]. Figure 15b shows the frequency dependence of R_s for the ZnSe/Si diode structure at the reverse bias voltage range (−4) to (−2.4) V by the step of 0.2 V. As shown in Fig. 15b, the value of R_s decreases with the increasing applied bias voltage at each frequency. Moreover, the values of R_s strongly depend on frequency and applied bias voltage. This behavior (the voltage and frequency dependence of R_s) could be attributed to the insulator layer and the distribution density of interface states [57].

4 Conclusion

In this work, In/n-ZnSe/p-Si/Al heterostructure was fabricated by e-beam evaporation technique at 200 °C substrate temperature. Also, to determine the material characterization of the deposited film layer, soda-lime glass substrates were used. The compositional structural analyses showed that the grown film was found in stoichiometric ratio and crystalized along (111) orientation direction. It was determined from AFM measurements that the surface of the film had crack and pinhole free behavior. As a result of transmission measurements, the optical band gap of the film was calculated as 2.8 eV. The current conduction mechanism across ZnSe/Si heterostructre was investigated by using temperature dependent forward bias I–V in the temperature interval of 220–360 K. It was found that as the zero-bias barrier height $\emptyset_{b0}$ and reverse saturation current I_0 were increasing, the ideality factor n was decreasing with the increasing temperature. This current behavior was assumed to be dependent on especially interfacial layer, interfaces states and series resistance. From the analysis of the possible current transport mechanism in the junction, the non-ideal forward bias I–V behavior were modeled by the anomaly in TE method. The obtained anomaly in TE theory was also studied on the evidence of a Gaussian distribution of the barrier height. Moreover, modifying I–V relation under the assumption of Gaussian theory, the value of the Richardson constant were obtained as 32.2 A/cm^{2}K^2, which was consistent with the reported works. The frequency dependent C–V and G/w–V at room temperature were found by the indication of interfacial states. The interface states densities D_{it} values were calculated and found in decreasing behavior with increases in frequency. Furthermore, voltage and frequency dependencies of series resistance of ZnSe/Si structure were analyzed.

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